CCD412
512 x 1024 Pixel Image Area
Frame Transfer CCD Image Sensor

FEATURES

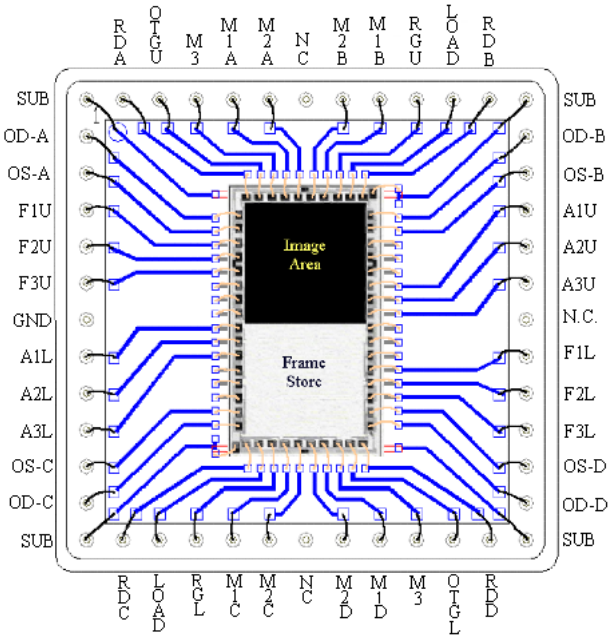
- **512 x 1024 Photosite CCD Array**
- **15 µm x 15 µm Pixels**
- **15.36mm x 15.36mm Image Area**
- **Frame Transfer Architecture**
- **100% Fill Factor**
- **Three Phase Buried Channel NMOS**
- **Multi-Pinned Phase (MPP) Operation**
- **Readout Noise Less Than 4 e^- at 50k pixels/sec**
- **4 Output Amplifiers**
- **Space Qualified**

GENERAL DESCRIPTION

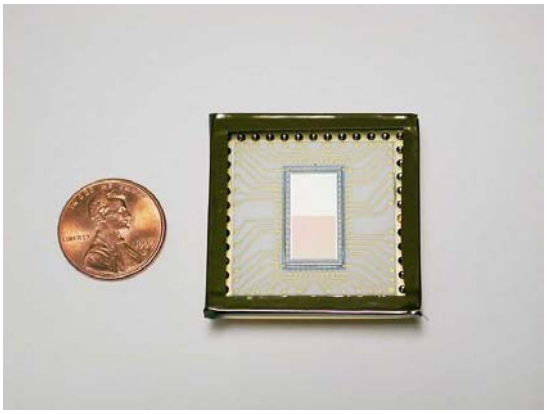
The CCD412 is a 512 x 1024 active element solid state Charge Coupled Device (CCD) Frame Transfer sensor. This CCD was designed specifically for space applications. The CCD412 is organized as an array of 512 horizontal by 1024 vertical imaging elements. The image area is 512 x 512. The pixel pitch is 15µm with a 100% fill factor. Three-phase clocking is employed in the imaging area as well as in the serial readout registers. The device is configured in a frame transfer architecture with the image area and frame store area defined by optical shielding. This frame transfer architecture allows high frame rate operation. Bussing of the parallel and serial clocks shall allow for imaging in either the top or bottom half of the parallel register with readout through one or two output ports, or imaging in the central half of the parallel register with read-out in four-quadrant format through four output ports. The device includes a temporary window (as shown in photo at right).

The output amplifiers feature a two-stage source follower design. The nominal read noise of the low-noise and high-speed output amplifiers is respectively 3.6 e^- and 4.8 e^- at a pixel rate of 50 kHz.

The CCD412 is normally available mounted in a solid-sidewall Kovar tub package with 48-pins.



CCD Package Configuration



CCD412 Mounted in a Kovar Package

FUNCTIONAL DESCRIPTION

The following functional elements are illustrated in the block diagram:

Image Sensing Elements: Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photoelectrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

The photosite structure is made up of contiguous CCD elements with no voids or inactive areas. In addition to sensing light, these elements are used to shift the image signal vertically. As a consequence, the device needs to be shuttered during readout.

Vertical Charge Shifting: The frame storage architecture of the CCD412 provides video information as a single sequential readout of 512 lines containing 512 photosensitive elements. At the end of an integration period, the ϕV_1, ϕV_2, and ϕV_3 clocks are used to transfer charge vertically through the CCD array to the horizontal readout register. Vertical columns are separated by a channel stop region to prevent charge migration. The image area is divided into an upper and lower half. Each 512 x 512 halve may be clocked independently or together.

The Vertical Transfer Gate (ϕVTG) is the final array gate before charge is transferred to the serial horizontal shift registers. For simplified operation ϕVTG may be tied to ϕV_3.

Horizontal Charge Shifting: ϕH_1, ϕH_2, and ϕH_3 are polysilicon gates used to transfer charge horizontally to the output amplifiers. The horizontal transport register is twice the size of the photosite to accommodate vertical binning. In binned mode, the array can be operated normally at full resolution, as a 512 x 512, 512 x 256, 256 x 256 or some other resolution. The charge may be read out through one, two or four amplifiers.

The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 20 additional register cells between the first pixel of each line and the output gate. The output from these locations contains no signal and may be used as a dark level reference.

The last clocked gate in the horizontal registers is twice as large as the others and can be used to horizontally bin charge. This gate requires its own clock, which may be tied to ϕH_3 for normal full

resolution readout. The output video is available following the high to low transition of ϕSG.

The reset FET in the horizontal readout, clocked appropriately with ϕR, allows binning of adjacent pixels.

Output Amplifier: The CCD412 has an output amplifier at each end of the horizontal registers for a total of four output ports. They are dual-stage floating diffusion amplifiers with a reset MOSFET tied to the input gate.

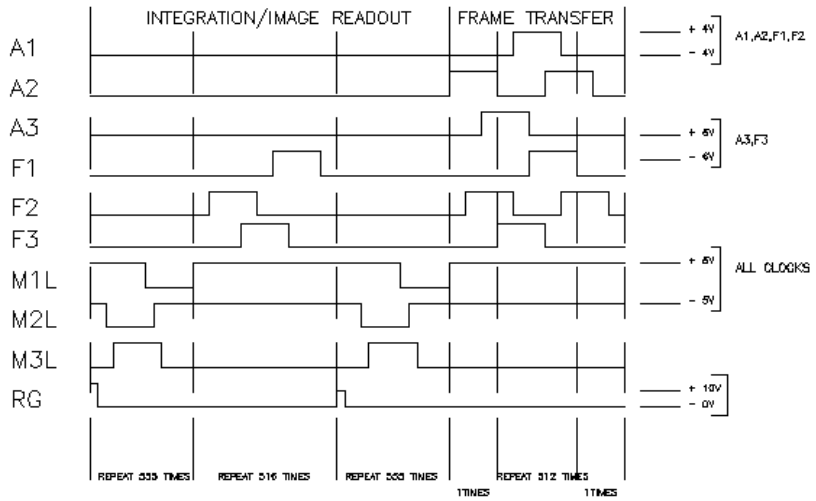
DEFINITION OF TERMS

Charge-Coupled Device A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Vertical Transport Clocks ϕV_1, ϕV_2, ϕV_3 the clock signals applied to the vertical transport register.

Horizontal Transport Clocks ϕH_1, ϕH_2, ϕH_3 the clock signals applied to the horizontal transport registers.

CCD412 TIMING DIAGRAM (One port timing – output C shown)



A1=A1U+F1U A2=A2U+F2U A3=A3U+F3U
F1=F1L+A1L F2=F2L+A2L F3=F3L+A3L

Charge packets are clocked to a pre-charged capacitor whose potential changes linearly in response to the number of electrons delivered. This potential is applied to the input gate of an NMOS amplifier producing a signal at the output V_{out} pin. The capacitor is reset with ϕR to a pre-charge level prior to the arrival of the next charge packet except when horizontally binning. It is reset by use of the reset MOSFET.

The output amplifier drain is tied to VDD. The source is connected to an external load resistor to ground. The source constitutes the video output from the device.

Multi-Pinned Phase: MPP is a CCD technology, which significantly reduces the dark current generation rate. CCDs are endowed with this capability by the addition of an ion implant step during the semiconductor manufacturing process.

This implant creates a virtual well in the array, which allows charge integration while maintaining pixel integrity with the Vertical clocks in the low state. Leaving the Vertical clocks in the low state during the integration cycle is the method used to implement MPP mode.
A drawback to utilizing the MPP mode is reduced full well capacity. The virtual well created by MPP implant does not hold as much charge as the normal buried channel operating mode which leaves one Vertical clock in the high state during integration. The CCD447 may be operated in the conventional buried channel mode with an increase in charge capacity over the MPP mode.

Reset Clock ϕR the clock applied to the reset switch of the output amplifier.

Dynamic Range The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

Saturation Exposure The minimum exposure level that produces and output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Responsivity The output signal voltage per unit of exposure.

Spectral Response Range The spectral band over, which the response per unit of radiant power is, more than 10% of the peak response.

Photo-Response Non-Uniformity The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

Dark Signal The output signal in the dark which is caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

Vertical Transfer Gate ϕVTG Gate structures adjacent to the end row of photosites and the horizontal transport registers. The charge

packets accumulated in the photosites are shifted vertically through the array. Upon reaching the end row of photosites, the charge is transferred in parallel via the transfer gates to the horizontal transport shift registers whenever the transfer gate voltage goes low.

Pixel Picture element or sensor element, also called photoelement or photosite.

Device Architecture

Array Size	1024 x 512	Image and Frame Storage
Pixel Size	15µm x 15µm	
Serial Register	Two	One top and one bottom
Serial Pixels	552	20 extended at each output
Output Ports	Four	Two for each serial mux
Output Amplifiers	Two stage	SEL immunity in mind
Optical Shield	Over frame store and serials	
Optical Density	$\geq$3	400-5000nm
Shield Alignment	$\pm$ 5 microns	Between rows 512 & 513

Performance Characteristics

Quantum Efficiency	30% - 34%	500-900um
Dark Current	$\leq$ 10pA/cm^2 @ -10°C	
High Frequency Dark Signal Non-Uniformity	$\leq$ 25 electrons rms @ -10°C	
Low Frequency Dark Signal Non-Uniformity	$\leq$ 25 electrons rms @ -10°C	
Hot Pixels	$\leq$ 100 @ -10°C	>10x ADS
Hot Columns	$\leq$ 100 @ -10°C	> 10 hot pixels
Read Noise	$\leq$ 45e- @ 25°C	RMS
Full Well Capacity	> 85ke	
Conversion Gain	$\geq$ 3.0µV per electron	
High Frequency PRNU	$\leq$ 5% rms	
Dark Pixels	$\leq$ 500	$\leq$ 20% of average response
Dark Columns	$\leq$ 10	
Spacing Between Dark or Defective Columns	$\geq$ 25	
Vertical CTE	$\geq$ 0.99995 per transfer	60k electrons, EPER
Horizontal CTE	$\geq$ 0.99995 per transfer	60k electrons, EPER
Vertical CTE	$\geq$ 0.99995 per transfer (-10°C)	6k electrons, Cd 109
Horizontal CTE	$\geq$ 0.99995 per transfer (-10°C)	6k electrons, Cd 109
Nonlinearity	$\leq \pm$ 3%	

Electrical Characteristics

DC Biases	$\leq$ 24 Volts	Goals: OD=22, OTG=+1V, RD=15V, LD=4.2V
Clock Levels	All between $\pm$ 10 volts	Goals: +4V, -8V ph 1&2, +6V, -8V ph3, +5V, -5V horizontal
Clock Timing	$\leq$ 20nsec rise and fall times	
DC Resistance	10 Mohm isolation	
Amplifier Bias Current	5 mA max	
Output Impedance	$\leq$ 2kohms	
Array Power Dissipation	$\leq$ 50mW with 3lohn load	One output
Gate Capacitance	5000$\pm$500pF Image or Storage 150$\pm$15pF Serial	Per Phase
Operating Temperature	-55°C to +125°C	
Storage Temperature	-65°C to +150°C	
Performance Temperature	-10°C to +40°C	Performance verification @ -20°C

QUANTUM EFFICIENCY ENHANCEMENT

All of our area array CCDs may be backside thinned for optimum QE. Incident light enters through the backside of the array, and since photons are not absorbed in the heavily doped polysilicon gate structures, the device quantum efficiency is optimized. In this configuration, the response at shorter wavelengths (400nm and below) is greatly enhanced.

COSMETIC GRADING

Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels and at different operating temperatures.

The CCD412 is available in several different grades, as well as custom selected grades. Consult Sales representative for available grading information and custom selections.

WARRANTY
Within twelve months of delivery to the end customer, Fairchild Imaging will repair or replace, at our option, any Fairchild Imaging camera product if any part is found to be defective in materials or workmanship. Contact Customer Service for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION
Fairchild Imaging certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specifications under which it is furnished.

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This product is designed, manufactured and distributed utilizing the ISO 9000:2000 Business Management System.