

PRELIMINARY

LORAL
Fairchild Imaging Sensors

CCD412
512 × 512 Element
Full Frame Image Sensor

FEATURES

- 512 × 512 Photosite Array
- 15 μ m × 15 μ m Pixel
- 7.68mm × 7.68mm Image Area
- 100% Fill Factor
- Multi-Pinned Phase (MPP) Option
- Readout Noise Less Than 7 Electrons
- Dynamic Range 10,000:1
- Single Output Channel
- Three Phase Buried Channel NMOS

GENERAL DESCRIPTION

The CCD412 is a 512 × 512 element solid state Charge Coupled Device (CCD) Full Frame area image sensor which is intended for use in high resolution scientific, industrial, and commercial electro-optical systems. The CCD412 is organized as a matrix array of 512 horizontal by 512 vertical CCD photosites. The pixel pitch and spacing is 15 μ m.

The imaging array may be operated in one of three modes, Buried Channel, Multi-Pinned Phase (MPP), and Surface Channel. The Buried Channel operation offers low noise performance and excellent charge transfer efficiencies. An additional implant under one vertical phase creates a virtual well which collects the photo-electrons with all Vertical clocks low during integration. This MPP mode decreases dark current down to 25 pA/cm² @ 25°C. The CCD412 may be operated in a Surface Channel mode, to increase full well capacity.

Excellent low noise performance is achieved by use of the buried channel CCD structure and a single stage low noise output amplifier.

Device processing is done using 2.5 micron design rules. The single metal, triple-poly process allows a photosite layout with smaller pixel geometries and fewer array blemishes.

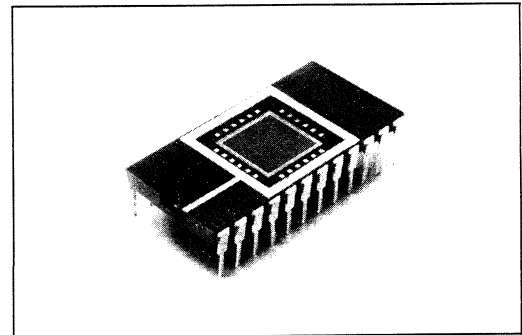
FUNCTIONAL DESCRIPTION

The CCD412 consists of the following functional elements illustrated in the block diagram.

Image Sensing Elements: Incident photons pass through a transparent polycrystalline silicon gate structure and are absorbed in the silicon crystal structure creating electron hole pairs. The resulting photo-electrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite in a linear function of the localized incident illumination intensity and integration period.

The photosite structure is made up of contiguous CCD elements with no voids or inactive areas. In addition to sensing light, these elements are used to shift image data vertically. Consequently, the device needs to be covered during readout.

Vertical Charge Shifting: The Full Frame architecture of the CCD412 provides video information as a single sequential



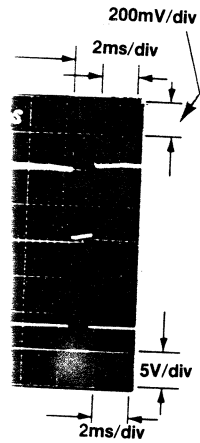
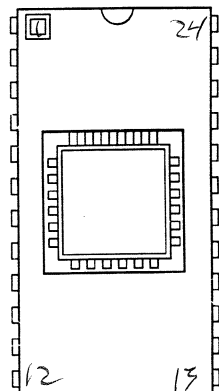
readout of 512 lines containing 512 photosite elements. At the end of an integration period the ϕV_1 , ϕV_2 , and ϕV_3 clocks, are used to transfer charge vertically through the CCD array to the horizontal readout register. Vertical columns are separated by a channel stop region to prevent charge migration.

The Vertical Transfer Gate (VTG) is the final array gate before charge is transferred to the serial horizontal shift registers. For simplified operation ϕVTG may be tied to ϕV_2 .

Horizontal Charge Shifting: ϕH_1 , ϕH_2 , and ϕH_3 are polysilicon gates used to transfer charge horizontally to the output amplifier. The horizontal transport register is twice the size of the photosite to allow for vertical binning. With binning the array can be operated normally at full resolution, as a 256 × 512, 256 × 256, or some other resolution.

PIN NUMBER/NAME PIN CONNECTIONS

1 ϕV_1	13 VIDEO _{OUT}
2	14 VSS
3 ϕV_3	15
4	16 ϕH_1
5	17
6 ATG ϕVTG	18 ϕH_2
7 VOG	19 ϕH_3
8	20
9 ϕR	21 ϕVTG
10 RDVRD	22
11	23
12 VDD	24 ϕV_2

REF.
24)10
54)

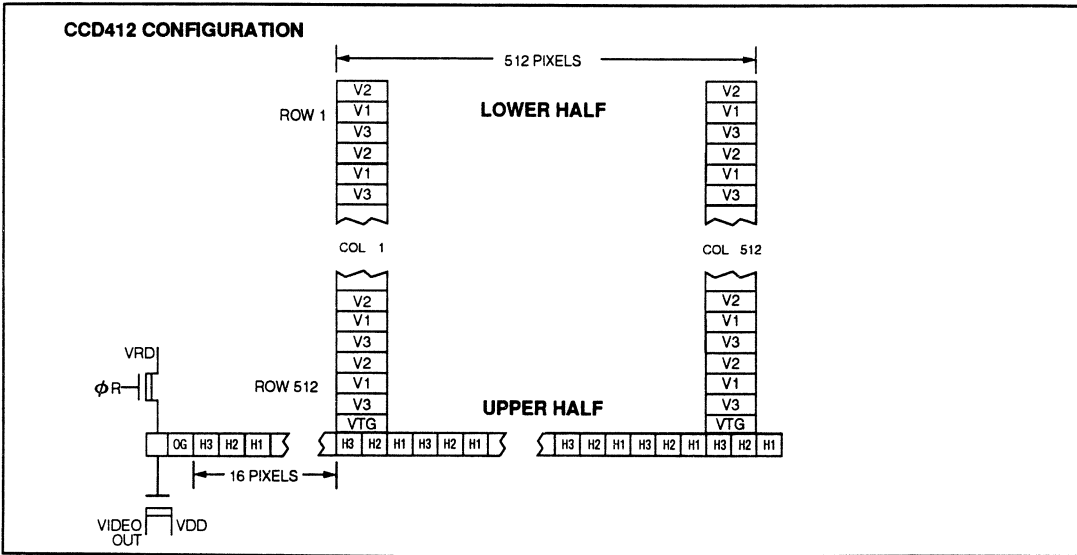
theses). Header is black
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products are carefully in-
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der which it is furnished.

g U.S. Patents:
17260; other patents

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The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 16 additional register cells between the first pixel of each line and the output amplifier. The output from these locations contain no signal and may be used as a dark level reference. The output video is available following the high to low transition of ϕ_{H3} .

The reset FET in the horizontal readout, clocked appropriately with ϕ_R , allows binning of adjacent pixels.

Output Amplifier: The CCD412 has one output amplifier at the end of the horizontal transport registers. It is a single FET floating diffusion amplifier with a reset MOSFET tied to its input gate.

Charge packets are clocked to a precharged capacitor whose potential changes linearly in response to the number of electrons delivered. This potential is applied to the input gate of an NMOS amplifier producing a signal at the output V_{OUT} pin. The capacitor is reset with ϕ_R to a precharge level prior to the arrival of the next charge packet except when horizontally binning. It is reset by use of the reset MOSFET.

The output amplifier drain is tied to VDD. The source is connected to an external load resistor to ground. The source constitutes the video output from the device.

Multi-Pinned Phase: MPP is a CCD technology which significantly reduces the dark current generation rate. CCDs are endowed with this capability by the addition of an implant during the semiconductor manufacturing process.

This implant creates a virtual well in the array which allows charge integration while maintaining pixel integrity with the Vertical clocks in the low state. Leaving the Vertical clocks in the low state during the integration cycle is the method used to implement MPP mode.

A drawback to utilizing the MPP mode is reduced full well capacity. The virtual well created by the MPP implant does not hold as much charge as the normal buried channel operating mode which leaves one Vertical clock in the high state during integration. The CCD412 may be operated in the conventional buried channel mode without any decrease in charge capacity.

DEFINITION OF TERMS

Charge-Coupled Device—A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Vertical Transport Clocks ϕ_{V1} , ϕ_{V2} , ϕ_{V3} —The clock signals applied to the vertical transport register.

Horizontal Transport Clocks ϕ_{H1} , ϕ_{H2} , ϕ_{H3} —The clock signals applied to the horizontal transport registers.

Reset Clock ϕ_R —The clock applied to the reset switch of the output amplifier.

Dynamic Range—The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4–6 times the RMS noise output.

Saturation Exposure—The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Spectral Response Range—The spectral band over which the response per unit of radiant power is more than 10% of the peak response.

Responsivity—The output signal voltage per unit of exposure.

Photo-Response Non-Uniformity—The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

Dark Signal—The output signal in the dark caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

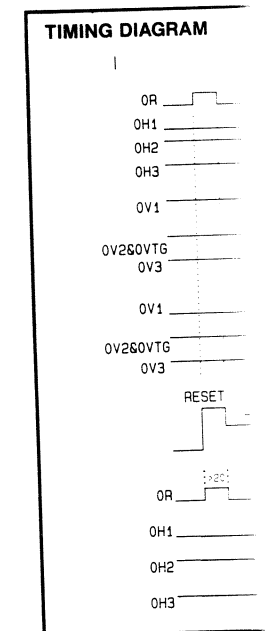
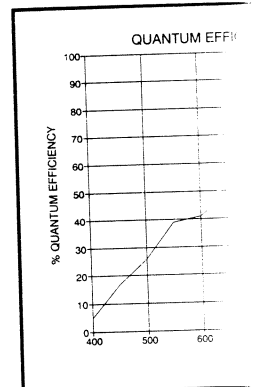
Vertical Transfer Gate ϕ_{VTG} —Gate structures adjacent to the end row of photosites and the horizontal transport registers. The charge packets accumulated in the photosites are shifted vertically through the array. Upon reaching the end row of photosites, the charge is transferred in parallel via the transfer

gates to the horizontal transport register gate voltage goes high.

Pixel—Picture element or photoelement or photosite.

Cosmetic Grading: Device grading for the image quality that are characterized as spurious with respect to neighboring elements determined in the dark, at various different device temperatures.

The CCD412 is available in as custom selected grades. grading information and cu

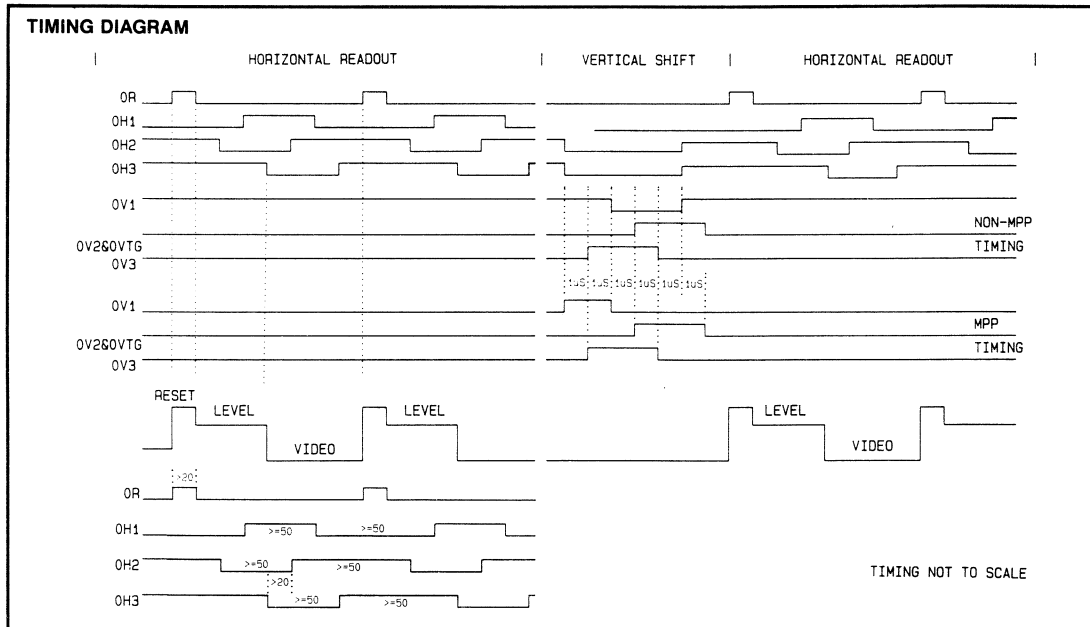
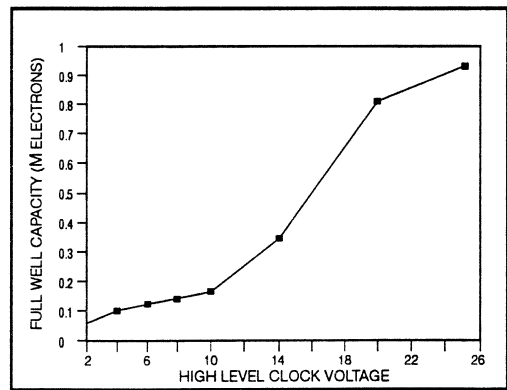
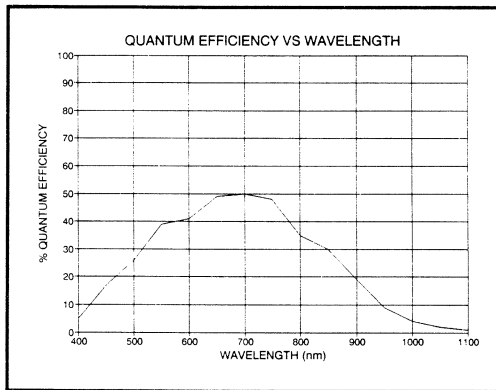
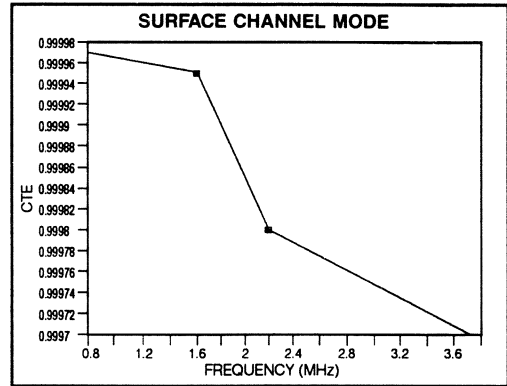


gates to the horizontal transport shift registers whenever the transfer gate voltage goes high.

Pixel—Picture element or sensor element also called photoelement or photosite.

Cosmetic Grading: Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels and for different device temperatures.

The CCD412 is available in various standard grades, as well as custom selected grades. Consult the factory for available grading information and custom selections.



PRELIMINARY

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DC OPERATING CHARACTERISTICS						
SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
V _{DD}	DC Supply Voltage		20.0		V	
V _{RD}	Reset Drain Voltage		13.0		V	
V _{OG}	Output Gate Voltage		1.0		V	
V _{SS}	Substrate Ground		0.0		V	

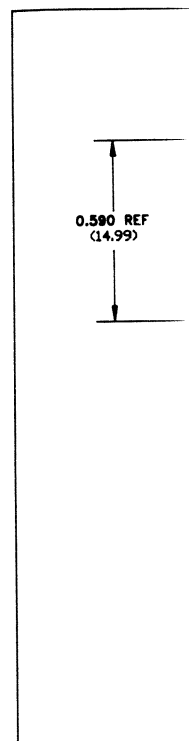
TYPICAL CLOCK VOLTAGES							
SYMBOL	PARAMETER	BURIED CHANNEL		SURFACE CHANNEL		UNIT	REMARKS
		HIGH	LOW	HIGH	LOW		
V ϕ _{H(1,2,3)}	Horizontal Clock	+5.0	-5.0	+16.0	0.0	V	Note 1
V ϕ _{V(1,2,3)}	Vertical Clock	+2.0	-8.0	+14.0	0.0	V	Note 1
V ϕ _R	Reset Clock	+8.0	0.0	+12.0	0.0	V	Note 1
V ϕ _{VTG}	Vertical Transfer Gate Clock	+2.0	-8.0	+14.0	0.0	V	Note 1

Note 1 ϕ H = 150pf, ϕ V = 5000pf. All clock rise and fall times should be > 10nSec.

AC CHARACTERISTICS MODE: Standard test conditions are nominal MPP clocks and DC operating Voltages, 1 MHz Horizontal Data Rate, 6 μ Sec Vertical shift cycle.						
SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
V _{ODC}	Output DC Level		14.0		V	
Z	Suggested Load Resistor		5.0	20	K Ω	

PERFORMANCE SPECIFICATIONS						
SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
V _{SAT}	Saturation Output Voltage	60		240	mV	Note 1
	Full Well Capacity	100,000		400,000	e ⁻	
	Output Amp Sensitivity	0.6			μ V/e ⁻	
PRNU	Photo-Response Non-Uniformity Peak-to-Peak		10		%V _{SAT}	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak			1.0	mV	
DC	Dark Current	0.025		2.0	nA/cm ²	Note 2
R	Responsivity		1.0		V/ μ Jcm ²	

Note 1 Maximum well capacity is achieved operating in Surface Channel mode, minimum capacity is in Buried Channel MPP mode.
 Note 2 Values shown are for 25°C. Dark current doubles for every 4-6° C.



CCD412

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Sensors

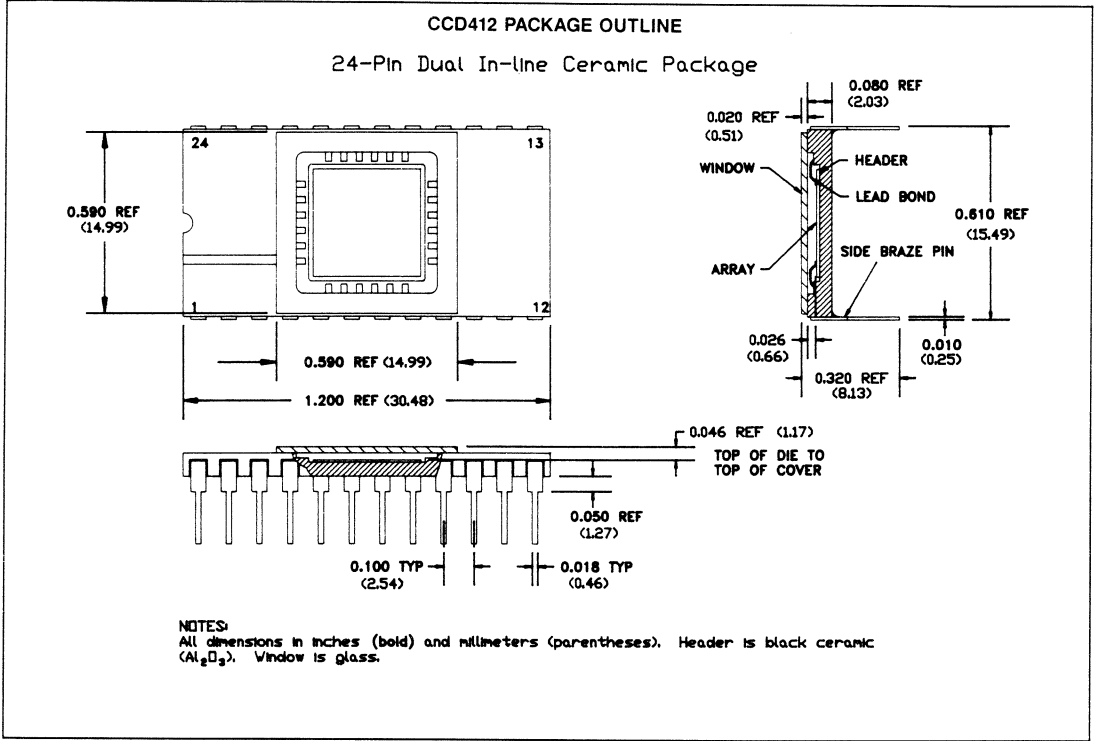
REMARKS

REMARKS
Note 1
Note 1
Note 1
Note 1

Voltages, 1 MHz

REMARKS

REMARKS
Note 1
Note 2



WARRANTY

Within twelve months of delivery to the end customer, Loral Fairchild will repair or replace, at our option, any Loral Fairchild camera product if any part is found to be defective in materials or workmanship. Contact factory for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Loral Fairchild Division certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specification under which it is furnished.



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