CALTECH CONTINUUM BACKEND
BACKPLANE CONNECTOR PINOUT DEFINITIONS
(OPEN ARCHITECTURE BUS ARRANGEMENT VER 3.0)

ROW #	COLUMN A	COLUMN B	COLUMN C
1	+5V (DIG)	SLOT ID 0	+5V (DIG)
2	+5V (DIG)	SLOT ID 1	+5V (DIG)
3	CFG SPARE 0	SLOT ID 2	CFG SPARE 1
4	JTAG TDI	SLOT ID 3	JTAG TDO
5	JTAG TMS	GND (DIG)	JTAG TCLK
6	/FORCE CFG	GND (DIG)	ALL CFG DONE
7	/OPER RESET	GND (DIG)	/SOFT RESET
8	SLAVE RESET	GND (DIG)	SLAVE CLOCK
9	SLAVE TEST	GND (DIG)	SLAVE DUMP
10	SLAVE START	GND (DIG)	SLAVE BLANK
11	SLAVE PHASE 0	GND (DIG)	SLAVE PHASE 1
12	ADDR 0	GND (DIG)	ADDR 1
13	ADDR 2	GND (DIG)	ADDR 3
14	ADDR 4	GND (DIG)	ADDR 5
15	ADDR 6	GND (DIG)	ADDR 7
16	/READ	GND (DIG)	/WRITE
17	< DATA 0 >	GND (DIG)	< DATA 1 >
18	< DATA 2 >	GND (DIG)	< DATA 3 >
19	< DATA 4 >	GND (DIG)	< DATA 5 >
20	< DATA 6 >	GND (DIG)	< DATA 7 >
21	< DATA 8 >	GND (DIG)	< DATA 9 >
22	< DATA 10 >	GND (DIG)	< DATA 11 >
23	< DATA 12 >	GND (DIG)	< DATA 13 >
24	< DATA 14 >	GND (DIG)	< DATA 15 >
25	< DATA 16 >	GND (DIG)	< DATA 17 (HB) >
26	MON SEL 0	GND (DIG)	MON SEL 1
27	MON SEL 2	GND (DIG)	SM /CFG DONE
28	SM /CFG ERROR	GND (DIG)	SM HEARTBEAT
29	VM 1.2V (DIG)	GND (ANA)	VM 2.5V (DIG)
30	VM 3.3V (DIG)	GND (ANA)	VM 5.0V (ANA)
31	+8V (ANA)	GND (ANA)	+8V (ANA)
32	+8V (ANA)	GND (ANA)	+8V (ANA)

NOTES

1) "< BUS DATA X >" IMPLIES BI-DIRECTIONAL DATA CAPABILITY

2) Only the four most significant bits of the address lines (ADDR 7, ADDR 6, ADDR 5, and ADDR 4) will be decoded using external logic. All other address lines (ADDR 3, ADDR 2, ADDR 1, and ADDR 0) may be viewed as general purpose "control lines" which originate at the MASTER FPGA and terminate at all four SLAVE FPGA's in parallel.

COLOR KEY

TEXT	DIGITAL GROUND "BUS"
TEXT	ANALOG GROUND "BUS"
TEXT	SLOT IDENTIFICATION PINS (HARDWIRED AT EACH CONNECTOR)
TEXT	+5 VOLT DIGITAL POWER SUPPLY "BUS"
TEXT	+8 VOLT ANALOG POWER SUPPLY "BUS"
TEXT	INSTRUMENT CONFIGURATION "BUS"
TEXT	INSTRUMENT RESET & HOUSEKEEPING "BUS"
TEXT	INTERNAL INSTRUMENT MONITORING "BUS"
TEXT	GENERAL PURPOSE FPGA INTERCONNECT "BUS"

07-SEP-04
-RLM-