The CCB external hardware interfaces

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Abstract

This document describes the principal characteristics of the external interfaces of the CCB, together with the internal properties that dictate them. It also describes the requirements that these characteristics place on the CCB interfaces of the GBT 1cm and 3mm differential radiometers.

Contents

List of Figures

Chapter 1

Overview

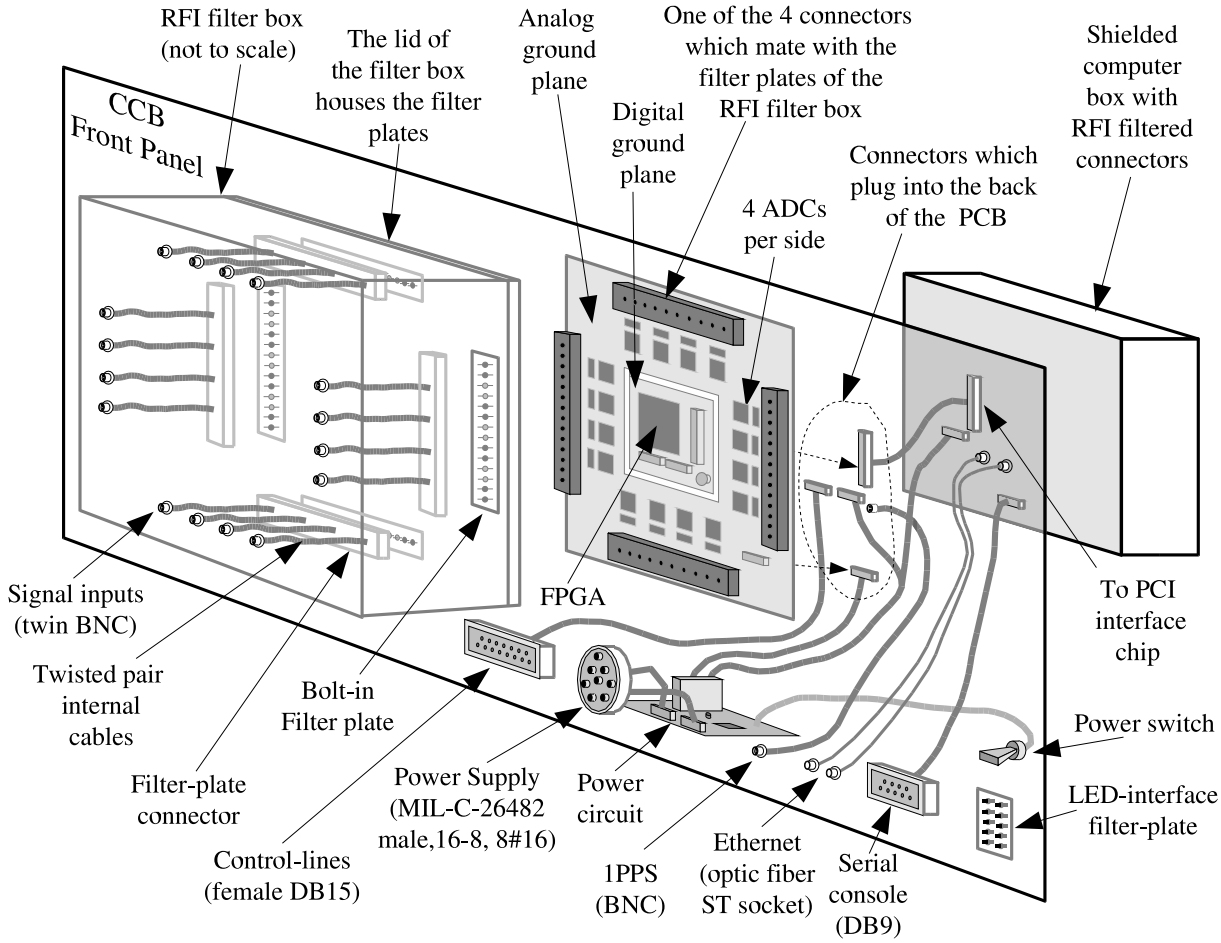

Figure 1.1: An rough outline of the main physical components of the CCB

The CCB will be enclosed in a shielding metal box, designed to screen against RFI emissions from the enclosed electronics, particularly the single-board embedded computer and the

FPGA. An outline of the front panel and the main components of the CCB that lie behind it, is shown in figure 1.1. In the diagram, the main components are shown disconnected and separated. Note that the internal computer box in this diagram, is a similarly shielded metal case, that will contain not only the embedded control computer, but also an ethernet optic-fiber media-converter, and a small PCB that interfaces the FPGA on the main PCB, to the PCI bus of the computer.

1.1 Connectors and cables

As shown in the figure, there will be 22 external connectors on the CCB front panel. These are discussed in detail in chapter 3, and summarized below, in table 1.1.

All of the sockets on both the internal computer box, and the main CCB case, have been selected for their RFI shielding properties, and all signals going through them are either low-pass filtered within the sockets themselves or, as shown for the signal inputs, within a well shielded internal filter box.

In the table, the specification of what type of cable, or cables, to use with the CCB power connector is marked as TBD. The reason for this is that this depends on what connectors will be used at the power-supply end of these cables, and this isn't clear yet.

Parameter	External Interface					
	Signals inputs	Control outputs	Power supplies	1-PPS input	Ethernet	Console
Connectors	16	1	1	1	2	1
Signals	16	4	5	1	2	4
Impedance (Ω)	78	100	–	50	–	–
Connector type	Twin-BNC	DB15	MIL-C-26482,16-8	RG108	ST	DB9
Socket gender	Female	Female	Male	Female	Female	Male
Plug gender	Male	Male	Female	Male	Male	Female
Cable type	Belden 9463	Belden 9806	–	RG58	fiber	–
Cable plug	89F2926†	571-7479084*	PT-06A-16-8P-SR*	227079-5*	–	571-7479054*
Metal backshell	–	571-7451722*	–	–	–	571-7451711*
Panel socket	13H4311†	56-715-005-JS◇	F64D16H8DN4103◇	228980-5*	–	657-56-705-005*
Cable	68H7813†	566-9806-100*	–	566-8259-100*	–	–

*– Mouser part number.
†– Newark Electronics part number.
◇– Spectrum Control part number.

Table 1.1: A summary of the external connectors and cables

It is assumed that the distance between the CCB and the corresponding receiver will be easily reachable by cables of no longer than 6 feet. The power cables, the 1PPS coax cable, and the ethernet fibers, on the other hand, can be any reasonable length.

1.2 The detected signals

Table 1.2 summarizes the required characteristics of the detected signals that the receiver sends to the CCB. The step-response settling time refers to the time taken for these signals to settle after a phase-switch transition, and is determined both by the response times of phase switches, and by the subsequent smearing/ringing effects of the low-pass filter. The low-pass filter time constant is a quantity used to determine the theoretical maximum SNR, as defined in section 2.1.1.

Constraint	Min	Max	Units
Step response settling time (to 0.04%)	0	1.0	μs
Phase-switching propagation-delay jitter	0	100	ns
Receiver low-pass filter attenuation at $\geq$ 10MHz	66	∞	dB
Receiver low-pass filter time-constant	0.5	0.1	μs
Common mode voltage	1.0	3.2	V
Differential voltage (no signal)	-2.5	-2.5	V
Differential voltage (max signal)	2.5	2.5	V

Table 1.2: A summary of the input signal requirements

As discussed in section 2.1.1, an 8-pole Bessel filter with a 3dB cutoff frequency of 2MHz, meets the time and frequency goals listed in this table.

1.3 Power supplies

Table 1.3 summarizes the anticipated power-supply requirements. The analog and digital power-supply needs will be met by separate power-supplies, with requirements that are elaborated in sections 2.4 and 2.5, respectively. The existing power supply in the receiver room doesn't have sufficient capacity to supply the needs of the CCB analog electronics, and it isn't authorized for use with digital electronics, so two new external power supplies will be needed for the CCB, one for the analog electronics, and another for the digital electronics. A third, 12V, power-supply may also be needed, depending on the type of embedded computer selected, and whether cooling fans are needed.

Origin	Voltage	Current	Comments
Analog PSU	5V	3A	–
Digital PSU	5V	8A	–
Digital PSU	12V	4A	(tentative)

Table 1.3: A summary of the power supply requirements

1.4 Cal-diode and phase-switch logic characteristics

Table 1.4 lists the characteristics of the differential opto-isolated digital signals that the CCB sends to the receiver to control the phase-switch and cal-diode switches.

Constraint	Min	Max	Units
Assumed rise time	0	100	ns
Assumed fall time	0	100	ns
Off differential voltage	-3.03	-2.25	V
On differential voltage	2.25	3.03	V

Table 1.4: A summary of the cal-diode & phase switch specifications

1.5 The Green Bank 1PPS signal

Table 1.5 lists the existing characteristics of the Green Bank 1-pulse-per-second signal. These are the values that will be assumed when designing the CCB time-stamp generator.

Quantity	Nominal value	Units
Pulse Period	1.0	s
Pulse width	1.0	μs
Pulse amplitude	4.0	V
Fall time	5.5	ns
Rise time	6.5	ns
Short circuit current	150	mA

Table 1.5: A summary of the assumed 1PPS properties

Chapter 2

Electrical properties

2.1 The properties required of the detected signals

2.1.1 Frequency and time-domain characteristics

- Phase-switched signal settling time: $\leq 1.0\mu$s

  Given essentially constant signals from the two arms of the radiometer, switching either of the phase-switches causes step-like changes in the signals going into the square-law detectors. In practice, because the phase-switches and the post-detector electronics will have finite rise times, and suffer from some degree of ringing and overshoot, the phase-switch transitions will take some time to settle to within the accuracy of measurement. During this interval, data will have to be discarded, so it is important that the its duration be minimized. Since the magnitude of the step response, within the linear operating region of the post-detector electronics, will be proportional to the magnitude of the input step, the worst-case time for the output to settle to within a particular absolute deviation from its final value, will occur for a step equal to the dynamic range of the system. Thus the worst case settling time, given an ADC providing 11 bits of dynamic range, is defined as the interval during which the output signal is more than $1/2^{11}$ of the dynamic range, from both the starting and ending values of the step.

  Note that the settling time does *not* include any fixed delays in the logic and cabling which drive the phase-switches, nor any fixed, frequency-independent delays in the signal path between the detectors and the CCB. These delays will be measured on an oscilloscope during initial tests, and thereafter passed by the manager to the CCB, to tell it what delays to use.

- Variability in the phase-switch propagation delay: ≤ 100ns

  Whereas constant delays between initiating and seeing the result of a phase-switch change, can be accommodated by the CCB logic, any jitter and thermal drifts in these

delays, can't. Any significant variability of this type, increases the duration over which the CCB must assume that the detected signals might still be in transition, and must therefore be added to the apparent settling time of the phase-switched signal.

- The attenuation at the 10MHz ADC sampling frequency: > 66dB

  This attenuation corresponds to the 2^{11} dynamic range of the A/D converter. This degree of attenuation is necessary because signals at this frequency are aliased to DC, and thus aren't averaged out by integrating multiple samples.

- The time-constant of the low-pass filter: $0.5\mu\text{s} \geq \tau > 0.1\mu\text{s}$

  At the outputs of the post-detector low-pass filters, the upper limit to the achievable SNR is given by the following equation.

$$\text{SNR} = \sqrt{B_{\perp}\tau} \tag{2.1}$$

  Where $B_{\perp}$ is a measure of the bandwidth of the pre-detector band-pass filters, and τ is a characteristic time-constant of the post-detector low-pass filters. These parameters are calculated according to the equations in [Rohlfs (2000)]. For an ideal square bandpass filter, $B_{\perp}$ is equal to the width of the square filter response, and since an approximately square bandpass is presumably the target of the receiver design, it is assumed that the numbers advertised for the channel bandwidths of the 3mm and 1cm receivers are close to their $B_{\perp}$ bandwidths. The value of τ depends on the form and order of low-pass filter chosen. For Bessel filters it is very roughly $0.5/f_{3dB}$, where f_{3dB} is the 3dB cutoff frequency of the filter.

  If the amplifiers and interface cables which follow the low-pass filters don't appreciably degrade the SNR, then equation 2.1 gives the SNR of the signals that reach the ADCs. When combined with the dynamic range of the ADCs, and the minimum system temperature expected, $\text{T}_{\text{sys}}^{\text{min}}$, this SNR dictates the range of signals that can be detected by the ADCs without saturating. Given an ADC with an effective resolution of n bits, from which q bits are allocated to sampling the noise of the minimum expected signal, the maximum total system temperature that can be measured without saturating the ADC, $\text{T}_{\text{sys}}^{\text{max}}$ is given by:

$$\text{T}_{\text{sys}}^{\text{max}} = 2^{(n-q)} \frac{\text{T}_{\text{sys}}^{\text{min}}}{\text{SNR}} \tag{2.2}$$

  After substituting equation 2.1, and rearranging the result, this becomes:

$$\frac{\text{T}_{\text{sys}}^{\text{max}}}{\text{T}_{\text{sys}}^{\text{min}}} = \frac{2^{(n-q)}}{\sqrt{B_{\perp}\tau}} \tag{2.3}$$

  This equation, which determines the dynamic range of the CCB, holds for values of τ greater than the 0.1μs ADC sampling period. The ADC that has been chosen for the CCB has over 11 bits of effective resolution, and the 3 least significant of these bits are

to be allocated to measuring the noise of the minimum detectable signal. Thus $q = 3$ and $n = 11$. In table 2.1 the advertised values for the bandwidths, $B_\perp$, of the 3mm and 1cm receivers, the corresponding estimates for the expected values of T_{sys}^{min}, and the values of T_{sys}^{max} which these estimates imply, are listed for a hypothetical 2MHz low-pass filter with $\tau = 0.5/f_{3dB} = 0.25\mu$s.

Note that the quoted values for T_{sys}^{min} are estimates of the system temperature when pointing the telescope at the zenith [Mason (2002)].

Receiver	Δf (GHz)	T_{sys}^{min} (K)	T_{sys}^{max} (K)
1cm	3.5	50	433
3mm	8.0	120	687

Table 2.1: The range of measurable system temperatures for $\tau = 0.25\mu$s

The choice of low-pass filter

The signal path between a given detector and the corresponding ADC includes a low-pass filter, various stages of amplification, impedance matching, and level shifting, as well as transmission over interface cables. Together these stages are required to behave like a low-pass filter that satisfies the above frequency and time requirements. In practice this means choosing a low-pass filter that satisfies these requirements, and then making sure that the other stages have much wider bandwidths and much shorter settling times than the low-pass filter.

To meet the settling time constraint, it turns out that it is necessary to use a low-pass filter that is optimized for its time response, rather than its frequency response. This means that a Bessel filter must be used. Table 2.2 lists the pertinent characteristics of practical 2MHz Bessel filters with varying numbers of poles. The laborious computation of these numbers is described in detail in Appendix A.

From this table one can see that for a white-noise input signal, an 8-pole 2MHz Bessel filter would meet all of the requirements, provided that the rise times of the phase switches and their driver electronics add up to no more than 0.3μs.

2.1.2 The signal levels of the detected signals

The detected output signals are to be transmitted in a balanced differential manner, with the following DC characteristics:

- The minimum common mode voltage: 1.0V

Poles	Attenuation (dB)			Settling time	DC Delay	τ
	2MHz	5MHz	10MHz	to 0.02% (μs)	(μs)	(μs)
1	3	8.6	14.1	0.68	0.08	0.16
2	3	12.7	23.9	0.63	0.11	0.22
3	3	16.3	33.1	0.70	0.14	0.23
4	3	19.3	41.6	0.66	0.17	0.24
5	3	21.3	49.2	0.74	0.19	0.24
6	3	22.5	55.9	0.73	0.22	0.24
7	3	23.0	62.0	0.71	0.24	0.24
8	3	23.0	66.4	0.70	0.25	0.24
9	3	22.0	70.0	0.69	0.27	0.24
10	3	22.4	75.1	0.68	0.29	0.24

Table 2.2: Important properties of 2MHz low-pass Bessel filters

- The maximum common mode voltage: 3.2V
- The differential voltage for no detected signal: -2.5V
- The differential voltage for the full-scale system-temperature: 2.5V

The maximum differential voltage should correspond to a total system temperature of T_{sys}^{max}, as given in table 2.1. Whereas ideally one would arrange for the weakest expected astronomical signal, T_{sys}^{min}, to generate the minimum differential voltage, it has been agreed that the detector output levels that are measured when the HEMT is turned off, will generate the minimum differential output. Although this represents up to a 5% loss in potential dynamic range, it does so to provide a welcome margin between the minimum expected signal and the negative saturation point of the ADC; and in practice, since the chosen ADC actually has one more bit of resolution than the 11 bits that the rest of this document relies on, the loss won't degrade the performance below the target specifications.

2.1.3 The maximum noise floor of the input signals

In section C.11, the theoretical input noise level from the receiver at which the sensitivity of the CCB would start to be degraded, was calculated to be $0.2\mu V/\sqrt{Hz}$.

2.2 The phase-switch and calibration-diode control signals

The phase-switch and calibration diode control signals are digital switching signals with required rise and fall times of no more than 100ns. As previously agreed, these signals will differentially drive the input stages of digital opto-isolators in the receiver. The output driver circuit of the CCB for one of these lines, plus the suggested receiving circuit in the receiver is shown in figure 2.1.

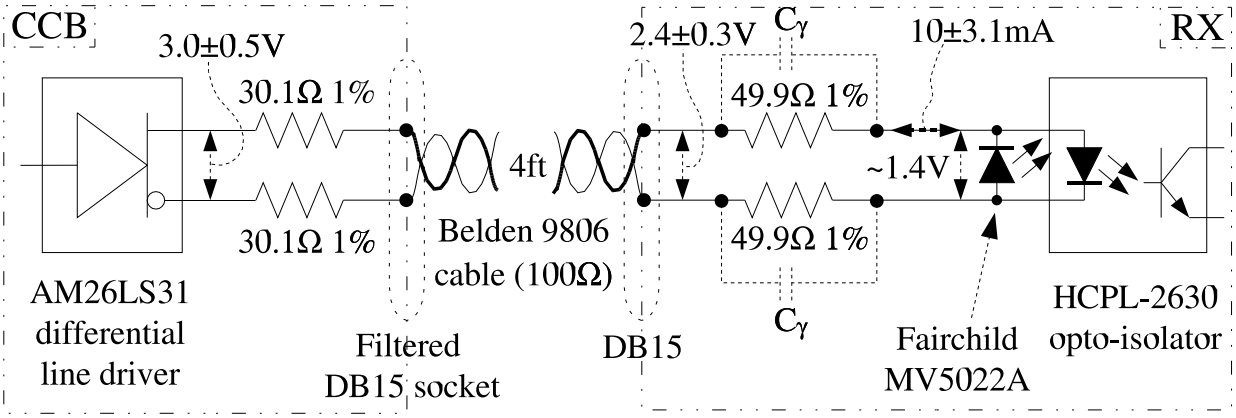

Figure 2.1: The schematic of one of the CCB/RX control lines

The control cable (see table 3.1) has a differential impedance of 100Ω, whereas the back-to-back LEDs which follow the cable have low impedances. Thus two 1% 49.9Ω resistors are placed in series with the two wires of each pair, in order to achieve a reasonable impedance match. In practice, the non-linear effects of the diodes and the RFI filters at the CCB end of the cable, could result in the signal being distorted. This is difficult to quantify, so it is suggested that initially the indicated circuit be adopted, but that the receiver PCB be laid out to accommodate the possibility of adding the pulse-shaping capacitors, C_γ, just in case they turn out to be necessary. These would be ceramic capacitors of no more than a few hundred pico-farads. Note that the resistors that follow the differential line driver in the CCB, are both to improve on the 1s short-circuit protection of the AM26LS31, and to produce a drive-current range appropriate for the opto-isolator LEDs. The indicated opto-isolator, HCPL-2630, and its dual equivalent, HCPL-2631, have TTL-compatible outputs, when powered from a 5V power supply, and their 75ns propagation delays meet the 100ns maximum rise time requirement. More details can be found in their combined data-sheet, at:

`http://www.fairchildsemi.com/ds/HC/HCPL-2630.pdf`

The MV5022A LED was selected for the closeness of its forward voltage at 10mA to the 1.4V forward voltage of the opto-isolator at the same current. Most LEDs have much higher

forward voltages than this, but according to the graph of forward-voltage versus current in the following data-sheet, the chosen LED has a typical forward voltage of about 1.4V at 10mA.

`http://www.fairchildsemi.com/ds/MV/MV5022A.pdf`

Its Newark part number is 34C1446.

2.3 The properties of the 1PPS signal

The 1PPS signal provided by Green Bank consists of a 1μs positive-going pulse, with a 4V amplitude, a rise time of about 6.5ns and a fall time of approximately 5.5ns. The existing GBT 1PPS driver is apparently short-circuit protected, with a maximum of 150mA output current.

Given that the minimum CCB integration time is 1ms, whereas the interrupt latency of the CCB's real-time OS will at best be around 10μs, and possibly as long as 100μs, the existing properties of the 1PPS signal are more than sufficient for the needs of the CCB.

2.4 The analog power requirements

The main components of the analog electronics in the CCB, are 16 ADCs and the 16 differential level-shifting amplifiers. The maximum current drawn by each of the AD9240 ADCs is documented as being 66mA at +5V. The AD8138 differential amplifiers are documented to draw up to 23mA from the single +5V supply. Thus, each analog input will need up to 89mA at 5V and 23mA at -5V. Since there are 16 inputs, this comes to a total of 1.4A at 5V. In practice there will be a few other components in the circuit, that haven't been specified yet, such as the voltage reference, so it probably makes sense to at least double this estimate and budget for 3A at 5V. Since 3A at 5V is the limit of the existing power supply in the receiver room, a new external power supply for the analog electronics will be required. At the ADC inputs, the full dynamic range of the input signals will span a differential range of 5V, sampled with a resolution of at least 11 bits. Thus the minimum signal sampled by the ADC will have a voltage of 2.4mV. The analog power supplies should have ripple voltages as small compared to these levels, as possible.

2.5 The digital power requirements

It is difficult to predict the power-supply needs of the digital electronics and the computer in advance. The main digital components are the CCB FPGA, the PCI interface chip, the single-board computer, and the UTP to 10Base-FL ethernet media converter.

- Apparently it isn't possible to make a safe prediction of the power consumption of an FPGA until its program has been written. However it is necessary to make some estimate now, in order to specify the power-supply interface connectors. An example of an FPGA implementation that is clocked much faster than the CCB FPGA will be, and also needs considerably more gates than the CCB should require, is the FPGA implementation in the Owen's Valley correlator. These FPGAs run at 125MHz, versus the CCB's 10MHz to 20MHz, and use 90% of the gates of a large FPGA. The result is a power consumption of 2.5W at 3.3V. This hopefully represents a pessimistic estimate of the amount of power needed by the CCB FPGA. Since other parts of the CCB digital electronics require 5V, the 3.3V needed by the FPGA will probably be derived from the 5V supply, which will raise the power drain to about 4.2W, unless a (radio-noisy) DC-DC inverter is used.

- The selected PCI interface chip, the PLX9054, draws a maximum of 250mA at 3.3V.

- There is a large, and ever-changing variety of SBCs (single board computers) available off the shelf, and each SBC has very different power requirements. Some need 5V, +12V and -12V, some also need 3.3V supplies, and a few conveniently only need a single 5V supply. The board that was originally proposed at the start of this project is no longer made, so a new target board has been tentatively selected.

  The *Cool RoadRunner III* SBC from Lippert, is a PC104+ format board, which supports Ultra-low-voltage mobile Pentium CPUs with speeds of 400MHz, 650MHz and 933MHz. At 650MHz this board only consumes 15.5W from a single 5V power supply, and purportedly doesn't need a CPU fan. This seems to be the fastest CPU that can currently be obtained without the need for active cooling, so this represents the minimum practical power consumption and cooling requirements for the CCB SBC.

  At the other end of the scale; in the extremely unlikely case that it turned out to be necessary to use an SBC with a Pentium 4 on it, running at 3.2GHz, Arbor's EmCore board draws 50W from the combination of 5V at 1.6A, 3.3V at 2A, and 12V at 2.8A, and needs a powerful CPU fan. Deriving the 3.3V supply from the 5V supply, using a 3-terminal regulator, would add 3.4W to the total power requirements. This represents the worst case power-supply and cooling requirements for the SBC.

- To convert the 100Base-TX twisted-pair ethernet interface of the single-board computer, to the 100Base-FX optic-fiber interface used at Green Bank, a media converter will be mounted within the shielded computer box. The converter that Green Bank generally uses, requires a 12V power supply input. This would require an extra power

supply if the RoadRunner CPU with its single 5V supply needs, were adopted, so instead the D-Link DFE-855 media converter will be used. This draws 1A at 5V.

Assuming that the 3.3V supplies were derived from the 5V supply using a 3-terminal regulator, rather than a DC-DC inverter, the worst case power supply requirements dictate a total power drain of 62W, partitioned between 5V at 5.75A, and 12V at 2.8A. For the more likely case of using the RoadRunner SBC, the total power consumption would only be 26W, from a single single 5V, 5.25A power supply. Obviously some headroom should be added to the above numbers, when selecting the actual power supplies. Note that if cooling fans for the CCB turn out to be necessary, a 12V 1A power supply will be needed, even if an SBC doesn't need 12V is used.

Chapter 3

Physical properties

3.1 The phase-switch and calibration diode control lines

3.1.1 Patch cables

As already documented, the four digital control lines differentially drive the input stages of opto-isolators in the receiver box. The distance between the CCB and receiver boxes is too short for crosstalk to be a serious issue, so it makes sense to bundle all of the twisted pair control lines within a single cable, with an overall shield. Although none of the control signals will switch at more than 25KHz, their digital transitions need to have rise times and fall times of no more than 100ns. This isn't a challenge as far as such a short cable goes, but it does require consideration when choosing filtered bulkhead connectors.

The control cable

To reduce RFI emissions, a multi-conductor twisted pair cable with both braid and foil overall shielding should be used. A suitable cable is given in table 3.1. This has an impedance of 100Ω.

Description	Mouser part #	Manufacturer #	Price
100ft, 4-pair, 100% foil + 90% braid shield	566-9806-100	Belden 9806	$63.28
DB15 metal backshell	571-7451722	AMP 745172-2	$8
Plug retainer screws	571-2059801	AMP 205980-1	$0.52
DB15 male plug	571-7479084	AMP 747908-4	$2.79

Table 3.1: Control cable parts

The control connector

For 4 differential pairs, a connector with at least 8 pins is needed. A DB9 connector would fulfill this, but wouldn't allow for the addition of unforeseen control lines in the future, so a DB15 connector will be used. The pin-out of the front panel connector is shown in figure 3.1.

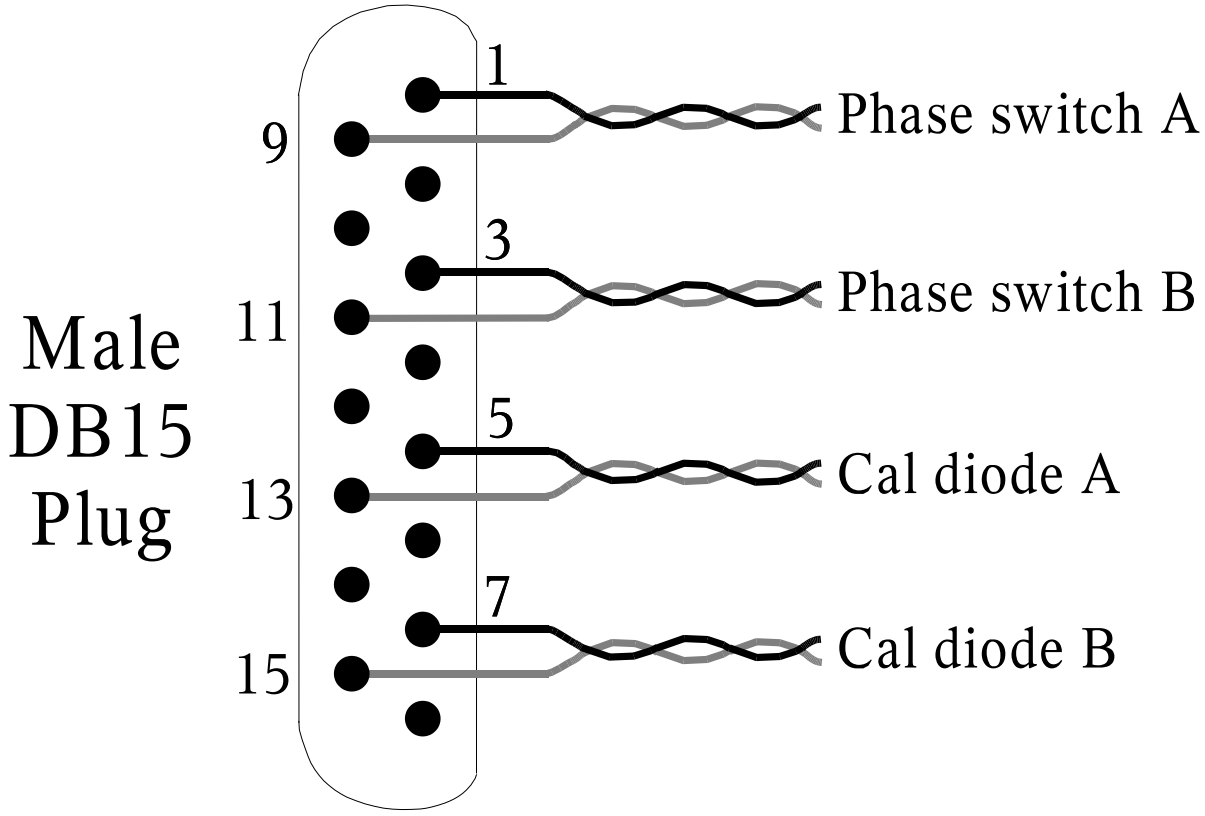

Figure 3.1: The pin-out of the DB15 plug of a CCB/RX control cable

Similarly, table 3.2 lists the chosen pins, but in addition, specifies explicitly the assignment of the wires within each twisted pair to the anodes and cathodes of the corresponding opto-isolators in the receiver box.

Anode pin	Cathode Pin	Control target
1	9	Phase-switch A
3	11	Phase-switch B
5	13	Calibration diode A
7	15	Calibration diode B

Table 3.2: The pin-out of the CCB/RX control-line DB15 connectors

The cable shown in table 3.1 has an outer diameter of 0.24 inches. The corresponding metal

die-cast backshell shown in the same table, is designed to clamp down on the outer shields of cables that have diameters in the range 0.24 to 0.30 inches, so this should be a good match. If, despite this specification, the chosen cable turns out to be too narrow to have its shield firmly clamped, the data-sheet for the backshell recommends that thinner cables have heat shrink tubing placed around their insulation, before the shield is folded back over it.

3.1.2 RFI filtered control-socket

To meet the RFI mitigation requirements for instruments housed in the GBT receiver room, the CCB box will have a filtered socket from `http://www.spectrumcontrol.com` to transmit the control signals. This will be a feedthrough DB15 bulkhead adapter with a female socket on the outside of the case, and a male socket on the inside of the case. According to the guidelines in the article at URL,

`http://www.spectrumcontrol.com/pdfs/edn.pdf`

to preserve a digital signal with rise times of t_r, the 3dB cutoff frequency of the low-pass filter should be no lower than $0.35/t_r$. Thus for the target rise time of 100ns the CCB control line filter must have a 3dB cutoff frequency of no more than 3.5MHz. To achieve reasonable attenuations at higher frequencies, a pi-section filter is required. The best matching pi-section filter that Spectrum Control sells has part number 56-715-005-JS. This has a worst-case 3dB frequency of 3.2MHz.

Description	Mouser part #	Manufacturer #	Price
Filtered DB15 bulkhead adapter	—	Spectrum Control 56-715-005-JS	?
Attachment hardware	571-205817-1	AMP 205817-1	$1.41

Table 3.3: Control socket parts

3.2 How the detected signals get from the receiver into the CCB

This section describes how detected signals are interfaced between the receiver and the CCB. One channel of the analog input circuit that implements the CCB end of this interface is described separately in appendix C.

3.2.1 The argument for using 16 individual cables

The original proposal was to use Infiniband connectors with Amphenol SkewClear cable. The reason for this was both because SkewClear cable was advertised to have very good crosstalk performance, whereas the crosstalk between a bundle of individual cables was hard to estimate, and because using one or two cables for all of the signals, instead of 16 individual cables would make things easier mechanically, and greatly ease set-up and tear-down. Unfortunately, this idea has had to be rejected, for the following reasons.

- Although the brochure for SkewClear cable indicates that the crosstalk in the cable is about -70dB below 100MHz, it doesn't say which of the many configurations of SkewClear cable this statistic referred to. Furthermore, this impressive performance is heavily dependent on outside influences, such as the way the line is driven. This is because the way that it is achieved is by matching the skew and impedance characteristics of the wires in each pair, to such a high degree, that when driven with perfectly balanced signals, the fields from the two wires cancel out to a high precision. Thus, if the signals driven onto these wires aren't perfectly balanced, then the crosstalk performance is correspondingly degraded. What this means is that to achieve the advertised performance, one needs not only well balanced drivers, but also well balanced RFI filters, good impedance matching of the connectors to the PCBs at each end, and connectors whose contacts magically resist differences in continuity from one pin to the next, caused by dirt and mechanical wear.

  In addition, there is no documentation of how much crosstalk the connectors add.

  In summary, the crosstalk that we could practically expect would probably be far lower than that advertised in the SkewClear brochure, which is already only marginally better than what is required by the CCB.

- Most Infiniband case-mounted sockets use latches to hold them in place, rather than screws. The result would be a poor continuity between the case and the metal shell of the connector, and thus poor RFI performance. Molex does make some that have screws, but the EMI gaskets behind them appear to leave gaps between their edges and the central metal guide, and thus don't appear to be sufficient for our needs.

- All of the available sockets seem to be of the surface mount variety, where one is expected to somehow solder the flat edges of protruding pins to the same side of the board as the connector sits on. This probably requires special equipment to do properly.

- The fact that building Infiniband patch cables requires special equipment, that they are of as-yet unproven reliability, and that Infiniband may turn out to be a short lived standard, means that we would have to buy a lot of up-front spares for the CCB.

- It was suggested that one could improve the crosstalk performance of SkewClear cable by only using half of the pairs, while grounding the intervening pairs. This ought to work for a flat cable, but unfortunately Infiniband connectors are only designed for

round cables, where each pair has many neighbors, not just two, so doing this wouldn't improve the crosstalk.

- Bundling multiple signals within a single cable prevents one from cross-wiring to cope with dead channels, or to debug a problem.

- Finally; actually finding suitable cables and sockets that could be bought in small numbers, proved to be a challenge, since most vendors are targeting manufacturers of high volume products.

For the above reasons, a solution that involves each of the 16 signals being delivered via individual shielded twisted pair cables will be used instead of Infiniband cables. Although the crosstalk performance of this can't be known in advance, if inter-cable crosstalk turns out to be a problem, the bundled cables can simply be held further apart, by running them through spacers.

3.2.2 Shielded individual twisted-pair cables for the signal lines

The obvious candidate for shielded individual twisted-pair cables is standard twinax. This is essentially a coaxial cable in which the center conductor is replaced with a twisted pair. Standard RG108 twinax cables only have a braid shield, which isn't very effective above 10MHz or so, so it is proposed that doubly shielded Belden 9463 cable be used instead. This has essentially the same diameter as RG108 cable, and has the same 78Ω impedance, but in addition to a braid shield with 55% coverage, it has a foil shield, with 100% coverage. The combination of using twisted pairs to reduce inductive coupling between neighboring cables, and double shields to reduce capacitive coupling, should result in low crosstalk between bundled cables.

Note that if 55% coverage for the braid part of the shield is considered too little, Belden part 9463F, is advertised to have 85% braid coverage. Unfortunately, this cable is sold in reels of at least 1000ft, whereas the proposed compromise cable (Belden 9463, without the F suffix) can be bought from Newark by the foot.

3.2.3 Twisted pair connectors for the signal lines

There are essentially two possible connector styles designed for RG108-style cables. One is a threaded connector, and the other is a BNC-style connector. The latter connector is the smaller of the two, and is easier to connect and disconnect, especially when 16 connectors have to be crammed together into a small area. Furthermore, AMP technical support was able to confirm that their twin BNC connectors are compatible with Belden 9463 cable. Thus Twin BNC connectors have been selected.

3.2.4 RFI filtering of the signal lines

There don't appear to be any off-the-shelf filtered twin-BNC connectors, so it will be necessary to build a custom RFI filtering solution. This can be accomplished by combining unfiltered twin-BNC connectors with separate RFI filters. Since the connections between the twin-BNC connectors and the RFI filters would otherwise provide a path for RFI to get in and out of the box, they will be enclosed within a separate shielded box, mounted to the inside wall of the CCB front panel. An outline of this box, and its contents, can be seen in figure 1.1. On one side of the box, where the box is bolted to the inner wall of the CCB, the bolts of the twin BNC bulkhead connectors will be traverse both the main case and the filter box. On the other side of the box, in its bolt-down lid, RFI-filtered feedthrough plates, from Spectrum Control, will mate with corresponding unfiltered connectors on the underside of the CCB main PCB.

As can be seen in figure 1.1, the 16 twin-BNC connectors will be arranged around the edges of a square, with 4 twin-BNC connectors on each side of this square. On the underside of the PCB, and the inner side of the filter box, there is a corresponding square arrangement of 4 edge connectors, each one serving 4 twin-BNC connectors. In principle, each edge connector needs at least 4×2 pins, since the signals are differential. In practice, since the separation between pins on a standard edge connector is only $0.1''$, and this could result in crosstalk between pins, as well as making connector assembly and circuit board layout more difficult, it makes more sense to use filter plates with some unused pins between each of the signal pairs. A filter plate with a single row of at least 14 pins would leave room for two unused pins ($0.3''$ of separation) between each of the 4 pairs.

Having taken so much trouble to specify low-pass filters with specific time domain and frequency properties for use in the receiver, we need to be careful not to choose RFI filters that degrade these properties. Since the filters in Spectrum Control's line of filtered connectors are poorly specified, are affected by impedance mismatches, and have unknown time-domain properties, the only way to ensure that they don't degrade performance is to choose a 3dB cutoff frequency that is significantly higher than the required 2MHz 3dB cutoff frequency. Table 3.4 lists the Spectrum Control part numbers of two 14-pin pi filters. These all have the same dimensions and mounting arrangements, but different cutoff frequencies. Note that the large range of 3dB frequency for each of these filters is due to poor component tolerances. It will require measurements on the bench to determine which of these filters meet the required time-domain response. Of the ones that do, the one with the lowest cutoff frequency will be selected.

Spectrum Control Part number	3dB cutoff frequency (MHz)	
	Minimum	Maximum
52-970-1-14-OC0	11	25
52-970-1-14-NC0	25	110

Table 3.4: Potential filter plates for the signal lines

3.2.5 Part numbers for the signal interface

Table 3.5 lists the part numbers of the signal cabling and connectors. Note that since it has now been decided that the twinax patch-cables will be ordered from a custom cable assembler, it won't be necessary to buy the expensive crimp tool which AMP sells, so this is no longer listed.

Description	Catalog #	Manufacturer #	Price
Twinax BNC plug	Newark 89F2926	AMP 332225-5	$19
Twinax BNC jack	Newark 13H4311	AMP 415832-1	$14
100ft twinax 9463 cable	Newark 68H7813	Belden 9463	$40
14-pin filtered plate	–	Spectrum Control 52-970-114-OC0	$32.64
14-pin filtered plate	–	Spectrum Control 52-970-114-NC0	$32.28
14-pin card connector	Mouser 649-68685-314	–	$3

Table 3.5: Part numbers for the CCB/RX signal cable and connectors

3.3 The 1PPS connector

The Green Bank 1-PPS signal will arrive at the CCB via a 50Ω RG58 coaxial cable, terminated with a male BNC connector. As suggested by John Ford, this will plug into a standard grounded female BNC bulkhead connector, with a ferrite bead threaded over the center conductor within the case.

3.4 External power supplies

3.4.1 The Analog Power Supply

The existing focus-room power supply doesn't have sufficient capacity to supply the needs of the CCB analog electronics, so a new external power supply will be needed. This should be a linear power supply, mounted along with the existing focus-room power supply, far enough away from the CCB to avoid magnetically inducing signals into the CCB's sensitive inputs. As elaborated in section 2.4, a power supply capable of supplying at least 3A at 5V, with as low ripple as possible, will be needed. A Lambda NNS155 power supply would provide 3A at 5V, with peak-to-peak ripple and noise voltages of 3mV. The catalog part numbers and price for this power supply are shown in table 3.6.

Description	Catalog #	Manufacturer #	Price
5V, 3A linear PSU	Arrow Electronics NNS155	Lambda NNS155	2×$382

Table 3.6: The analog power supplies

3.4.2 The Digital Power Supply

Currently the focus room does not provide a power supply that is suitable for powering digital electronics. It is thus proposed that a new linear power supply be bought for powering the CCB digital electronics, and that this should be mounted adjacent to the existing and new analog power supplies, far enough away from the CCB to not cause magnetically induced 60Hz interference.

Note that the alternative of placing a digital power supply within the CCB would be problematic. Linear and switch-mode power-supplies both generate strong extraneous signals that could be picked up by the sensitive CCB analog electronics. In the linear power-supply case, this would involve near-field 60Hz magnetically-induced pickup, whereas in the switch-mode case, it would involve wide-bandwidth switching noise. Embedding a linear power supply within the CCB would also significantly add to the amount of heat that had to be dissipated from the case, and thus increase the size of any cooling vents and fans. This would add to the likelihood of RFI leakage. An external, linear power supply, mounted away from the CCB would not cause these problems, either to the CCB, or to other instruments. The only danger would be that the power cables going through the wrap could radiate transients. In practice the CCB digital power supply lines will be well filtered to the chassis ground, as discussed below, so radiated transients are unlikely to be strong enough to be an issue, provided that the CCB case is well grounded. Note that shielding the power cable would have limited utility, since digital switching currents on power-lines are most likely to induce transients into neighboring conductors through magnetic induction, rather than radiated E-fields.

As discussed in section 2.5, it is most likely that a single 5V power supply will be needed, capable of comfortably supplying at least 5.25A. Alternatively, in the worst case considered, two 5V,5.75A and 12V,2.8A supplies will be needed. Since extremely low ripple and load regulation isn't needed for the digital power supplies, expensive Lambda power supplies, don't need to be used. The two linear, open-frame power-supplies shown in table 3.7, should be sufficient.

Description	Catalog #	Manufacturer #	Price
5V, 9A linear PSU	Condor HN5-9/OV-A++	Mouser 675-HN5-9OVA	$82
12V, 3.4A linear PSU	Condor HD5-12/OV-A++	Mouser 675-HD5-12OVA	$93

Table 3.7: The digital power supplies

Note that the current rating of the 12V power-supply is much higher than will be needed if

the 12V supply is only used for cooling fans. In that case a 12V,1A supply would do.

3.5 Power cables

The cables from the digital and analog power supplies will both terminate in a single connector that plugs into a filtered socket on the front panel of the CCB. The only sockets that Spectrum Control sells that appear to meet both the current-handling and RFI-filtering requirements of the CCB, are military standard power connectors. Among these, there are a number of possibilities, but only one seems to have a matching plug conveniently available from Mouser.

These are MIL-C-26482, series 1 connectors, with a shell size of 16, containing 8 size-16 pins. Each pin is capable of handling currents of up to 13A. A suitable Spectrum Control socket, armed with Pi-configuration low-pass filters on each pin, has part number F64D16H8DN4103. These filters have 0.5MHz 3dB cutoff frequencies, and insertion losses exceeding 64dB above 100MHz. The pin-out of the front-panel socket is shown in figure 3.2.

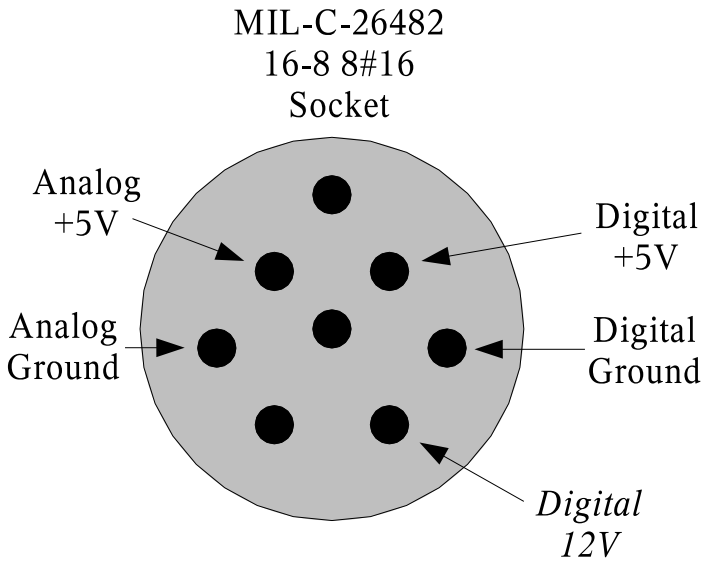

Figure 3.2: The pin-out of the CCB front-panel power-socket

The matching, unfiltered Amphenol plug from Mouser has part number, PT-06A-16-8P-SR.

Note that a power-supply connector mounted on the internal computer box, will also be filtered, to protect the analog electronics within the CCB from computer-generated RFI.

3.6 A front-panel and remote power switches

The CCB will effectively have two power switches, one on the front panel and a remote, momentary-action reset switch in the control room. The latter, which will only work when the main front-panel power-switch is in the *on* position, is designed for remote power-cycling of the CCB. When the remote operator presses the reset button, all power-supply inputs to the CCB will be abruptly cut. Then about 200ms after the operator releases the reset button, the power supply inputs will be restored, and the CCB will reinitialize itself. Since this reinitialization involves reloading the operating system and CCB software anew from flash firmware into a RAM-disk, file-system corruption due to cutting the power without first shutting down, shouldn't be a concern. On the other hand, the manager may want to have its connection to the CCB terminated cleanly first, so a remote shutdown command has already been included in the manager/CCB communications library.

Note that in order to meet EMI requirements, the toggle switch will have a metal lever and a threaded metal bushing attached to a metal backing plate.

The design of the power-management circuit, plus the corresponding list of parts is provided in appendix B.

3.7 Front panel indicator LEDs

To provide a basic sign-of-life indication, and to provide some clues when the CCB can't be reached over the ethernet, some indicator LEDs will be included. Potentially useful LEDs would include the following.

- A power-on indicator.
- An ethernet activity indicator.
- A disk activity indicator for the solid-state disk.

Since holes for mounting front panel LEDs would compromise the RFI shielding of the CCB, the LEDs will be mounted outside the case, and the signals reaching them will be filtered where they exit the front panel. To do this, a dual-row filtered plate from Spectrum Control will be used to get the signals through the CCB front panel. The pins on the outer side of this plate will be soldered to a short strip of veroboard, to which the LED leads will also be soldered. Some, yet to be determined, means to enclose all but the tops of these LEDs will then be added, both for protection and to make the result more aesthetically pleasing. On the inside of the case, for each LED, one Molex 2-position, 0.1 inch SL connector will be pushed onto the back pins of the filtered plate, with a crimped twisted-pair of wires going to the source of that LED's signal. Since the number of LEDs isn't currently known, a filtered

plate with 5 dual-row positions will be used. Suitable part numbers are shown in table 3.8. The filtered plate listed in the table is a bolt-in plate with 4MHz pi filters.

Description	Mouser Catalog #	Manufacturer #	Price
2×5-pin filtered plate	–	Spectrum Control 52-970-2-05-SA0	?
2-circuit SL connector	538-50-57-9002	Molex 50-57-9002	5 × $0.53

Table 3.8: Some parts for the LED indicator interface

3.8 Cooling

At this point it isn't known whether active cooling of any of the components will be needed or not. The FPGA programming and the choice of single board computer will determine this. If at all possible, fans will be avoided, for the following reasons:

- Their rotating magnetic fields could cause low-frequency pickup in the analog electronics.
- They necessitate an extra power supply, since motors put spikes on their power-lines.
- If fans are really needed, then their unpredictable finite lifetimes, would dictate the inclusion of remote CPU temperature monitoring, and alarms.

Regardless of whether fans are used or not, cooling vents will be included. These will provide some passive cooling in the event that fans aren't needed. There will be two vents in opposite sides of the main CCB box, and another two at either side of the internal computer box. The outer box vents will be suitable for standard 60mm size fans, while the computer box vents will be suitable for standard 40mm fans. Chomerics' CHO-CELL™ shielded vent panels will be used. Chomerics claims that these vents have shielding effectivenesses of 90dB up to 10GHz. Unfortunately, since they have to be made to order, part numbers and prices can't be provided here.

3.9 The ethernet connectors

Ethernet will enter and exit both the outer CCB case and the inner computer box, via pairs of ST bulkhead adapters.

These connectors are solid metal, apart from the 2.75mm hole through which the glass ferrule of the fiber connector on the outside of the case mates with that of the corresponding

Description	Catalog #	Manufacturer #	Price
ST bulkhead adapter	Newark 93F6596	Amphenol 953-122-5003	$4 \times \$6$

Table 3.9: Part numbers for the optic fiber ethernet interface

connector on the inside of the case. Since both of the patch cables will be chosen to have connectors with metal sleeves, it is hoped that the two metal plugs, together with the metal bulkhead connector between them, will form a sufficiently good RFI shield. If not, then one way to fix this would presumably be to solder a copper tube to the sleeve of the plug on the inside of the box to form a cutoff waveguide.

3.10 The console serial port plus reset line

Green Bank provides a 3-wire serial line for the console of each backend. The same cable is also used for reseting the backends, with pins 1 and 9 of the connector being connected to the two sides of a remotely controlled switch. In keeping with the conventions used on modern PCs, access to the serial port of the embedded computer is provided by a male DB9 socket on the front panel. The pinout of the corresponding female plug of the patch cable, is shown in figure 3.3.

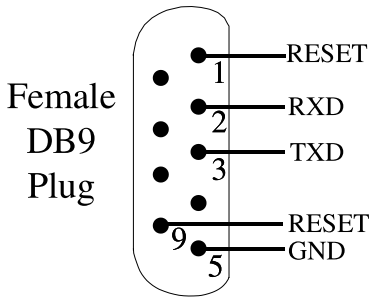

Figure 3.3: The console serial cable

3.10.1 Console front-panel socket

Following from other backends at Green Bank, the male DB9 socket will be a Spectrum Control 4000pF pi-filtered socket. For the CCB a bulkhead pin-socket adapter will be used in order to facilitate the use of a shielded patch cable within the CCB to connect the front-panel socket to an identical filtered adapter on the internal shielded computer box. This has the part number listed in table 3.10.

Description	Catalog #	Manufacturer #	Price
Bulkhead filtered DB9 adapter	Mouser 657-56-705-005	Spectrum Control 56-705-005	$38.50

Table 3.10: Part numbers for the console front-panel socket

3.10.2 Console cable

Part numbers for the female DB9 plug that plugs into the console socket, along with the corresponding cable, are shown in table 3.11.

Description	Mouser #	Manufacturer #	Price
DB9 metal backshell	571-7451711	AMP 745171-1	$6.27
Plug retainer screws	571-2059801	AMP 205980-1	$0.52
DB9 female plug	571-7479054	AMP 747905-4	$2.79

Table 3.11: Part numbers for the CCB end of the console-port serial cable

The backshell listed in the table, can accommodate shielded cables with outer diameters of between 0.21 and 0.24 inches.

Appendix A

Bessel filter computations

Since I was unable to find official tabulations of the time and frequency-domain characteristics of Bessel filters, I ended up having to calculate them myself. This appendix documents how I did this.

For the sake of example, whenever it makes sense to have a concrete example, calculations are performed in Matlab for a 3-pole Bessel filter. Starting from the tabulation of filter transfer functions on page 390 of [Su (2002)], one finds that the voltage transfer function of a 3-pole Bessel filter has the following equation:

$$H(s) = \frac{15}{s^3 + 6s^2 + 15s + 15} \tag{A.1}$$

where s is the complex frequency $i\omega$. As will be explained later, all of the Bessel-filter transfer functions listed by [Su (2002)], are *delay-normalized*.

As indicated on page 26 of [Su (2002)] the power transfer function corresponding to the voltage transfer function $H(s)$ is given by,

$$|H(s)|^2 = H(s)H(-s). \tag{A.2}$$

In Matlab this can be computed symbolically, by typing:

```
syms s;
top=15;
bot=(s^3 + 6*s^2 + 15*s + 15);
hh = top*top/(expand(bot * subs(bot, s, -s)))
```

where the `subs()` function is used to substitute $-s$ for s in the symbolic equation in `bot`. The result is,

$$|H(s)|^2 = \frac{225}{-s^6 + 6\,s^4 - 4\,s^2 + 225}. \tag{A.3}$$

A.1 Frequency normalization

It is conventional to tabulate the polynomial coefficients of most types of low-pass filters such that the resulting filters have 3dB cutoff frequencies of $1\text{rad}\,s^{-1}$. Such filters are referred to as being frequency-normalized. The equivalent coefficients for a filter that is of the same type and order, but has a different cutoff frequency, ω_{3dB}, can then be calculated by multiplying the polynomial coefficients of the individual ω^n terms by $1/\omega_{3dB}^n$.

If a frequency-normalized filter is found to have a desired property at a particular frequency, a filter with a different 3dB cutoff frequency will have the same property at ω_{3dB} times this frequency. Similarly, if a frequency-normalized filter takes a certain amount of time to respond to an event in the time domain, the amount of time that a similar filter with a different 3dB cutoff frequency will take to respond in the same way, will be $1/\omega_{3dB}$.

Unfortunately, since Bessel filters are designed for their time-domain delay properties, their polynomials usually refer to delay-normalized filters, rather than frequency-normalized. This is inconvenient, since filter manufacturers generally design filters for specific 3dB cutoff frequencies. Fortunately, as should be evident from the previous paragraph, conversion between delay-normalized and frequency-normalized filter-polynomials simply involves scaling the coefficients of the individual ω^n terms by Ω_{3db}^n, where Ω_{3db} is the 3dB cutoff frequency of the delay-normalized filter, expressed in $\text{rad}\,s^{-1}$.

To perform this renormalization, one first needs to know the 3dB cutoff frequency of the target filter (ie. Ω_{3dB}). Based on equation A.3, one can solve for the 3dB cutoff frequency of a 3-pole, delay-normalized Bessel filter by typing the following into Matlab.

```
solve('225/(-s^6+6*s^4-45*s^2+225)=0.5')
```

or equivalently, by using the previous definition of the symbolic `hh` variable, one could type:

```
solve([char(hh) '=0.5'])
```

In both cases matlab has been asked to solve for the value of s at which the power-transfer function of equation A.3 is reduced to half of its unity DC value. Matlab returns a number

of complex solutions, but since $s = i\omega$, where ω is real, and the transfer function has to be symmetric about $s = 0$ to keep the output signal real, the desired solutions of s must be a pair of purely imaginary values that have the same magnitude as each other, but opposite signs. Indeed the only purely imaginary solutions have identical magnitudes of $1.756\,\mathrm{rad}\,s^{-1}$ and opposite signs. Thus the frequency renormalization factor to convert a delay-normalized 3-pole Bessel filter to a frequency-normalized Bessel filter of the same order, is:

$$\Omega_{3db} = 1.756\,\mathrm{rad}\,s^{-1} \tag{A.4}$$

In Matlab this can be used to convert the delay-normalized power transfer function `hh` to a frequency-normalized power-transfer function, `hhf`, by typing:

```
hhf = subs(hh, s, 1.756*s);
```

Remembering that $s = i\omega$, one can then confirm that at $\omega = 1\,\mathrm{rad}\,s^{-1}$ the frequency-normalized power transfer-function has a gain of 0.5 by typing:

```
subs(hhf, s, 1.0*i)
```

Matlab reports that the result is 0.5 (ie. 3dB), as expected. Similarly, to work out the value at 5 times the cutoff frequency, and convert this to dB, one would type:

```
10*log10(subs(hhf, s, 5.0*i))
```

which yields -33.45dB.

A.2 Computing the group delay of a Bessel filter

Bessel filters are designed to present a delay that is as constant as possible from DC to an order-dependent multiple of the cutoff frequency. The group delay at DC is the standard measure of this delay, and is given by

$$Delay = -\frac{d\theta_{\omega=0}}{d\omega} \tag{A.5}$$

Where θ_ω is the phase of the transfer function at frequency $\omega\,\mathrm{rad}\,s^{-1}$. To compute this, first note that all Bessel filter transfer functions have the form:

$$H(\omega) = \frac{C_0}{\sum_{n=0}^{N} C_n (i\omega)^n} \tag{A.6}$$

where the C_n are the constant coefficients of the denominator polynomials. At $\omega \simeq 0$, one can discard all terms in this equation except the ω^0 and ω^n terms, which leaves:

$$H(\omega \simeq 0) \simeq \frac{C_0}{iC_1\omega + C_0} \tag{A.7}$$

Multiplying the top and bottom of this equation by the complex conjugate of the denominator, one gets:

$$H(\omega \simeq 0) \simeq \frac{C_0\,(C_0 - i\,C_1\,\omega)}{C_0^2 - C_1^2\,\omega^2} \tag{A.8}$$

The phase of the transfer function is thus given by:

$$\tan\theta_{\omega \simeq 0} \simeq \frac{-C_1\,\omega}{C_0} \tag{A.9}$$

Thus, for $\omega \ll \frac{C_0}{C_1}$, the phase is simply the right hand side of this equation, and the group delay given by equation A.5 is,

$$Delay \simeq \frac{C_1}{C_0} \tag{A.10}$$

Now if one examines the Bessel filter polynomial coefficients given in [Su (2002)], it turns out that in all cases $C_0 = C_1$. Thus for these filters, the DC group delay is always 1s. This tells us that the tabulated polynomials refer to *delay-normalized* Bessel filters. To convert these polynomials to represent frequency-normalized Bessel filters, one simply scales the C_n terms by Ω_{3db}^n, where, as noted above, $\Omega_{3db} = 1.756$ for a 3-pole Bessel filter. Thus one finds that the DC group-delay is Ω_{3db} seconds for a frequency-normalized Bessel filter, and for Bessel filters with other 3dB cutoff frequencies, ω_{3dB}, it is

$$Delay = \frac{\Omega_{3db}}{\omega_{3dB}}. \tag{A.11}$$

Note that the delays calculated in this way agree with the subset of delays that are given by [Daniels (1974)].

A.3 Computing the settling time of a Bessel filter

In order to compute the settling time of the filter to a specified accuracy, one first has to compute the inverse Laplace transform of the product of the voltage transfer function of the filter and the Laplace transform of a unit step-function input signal. The result is the time response of the filter to a unit step-function input at time $t = 0$.

Tables of standard Laplace transforms indicate that the Laplace transform of a step-function is $1/s$. Multiplying equation A.1 by this, one gets:

$$H(s)/s = \frac{15}{s^4 + 6s^3 + 15s^2 + 15s + 0} \tag{A.12}$$

Unfortunately the Matlab `ilaplace()` function isn't able to compute the inverse Laplace transform of this, so one is forced to do the inverse transform partly by hand. This is done by first determining the partial fraction expansion of equation A.12 and then using tables of standard Laplace transforms to determine the sum of the inverse Laplace transforms of each of the resulting roots. Fortunately Matlab provides the `residue()` function to perform the expansion. For the 3-pole delay-normalized Bessel filter this is done by typing:

```
[res,pol,fdth] = residue(15, [1 6 15 15 0])
```

Where the two arguments of the `residue()` function are vectors of the polynomial coefficients of the numerator and denominator polynomials of equation A.12. The coefficients are presented in descending order of the n's in $C_n\, s^n$.

The `res` and `pol` return values are vectors of the residue-coefficients and complex frequencies of each of the poles of this equation. Given a root of residue R and complex frequency P, the Laplace transform is given by $R\, e^P$, where both R and P are complex. Applying this to each of the poles returned by the above `residue()` call and summing the results, one finds that the voltage response of a 3rd order delay-normalized Bessel filter to an input step function is given by:

$$v(t) = (0.4753{+}0.7928\,i)\, e^{(-1.8389+1.7544\,i)\,t} + (0.4753{-}0.7928\,i)\, e^{(-1.8389-1.7544\,i)\,t} - 1.9507\, e^{-2.3222\,t} + 1 \tag{A.13}$$

Examining this equation one notes that two of the pole frequencies are complex conjugates of each other, so by using the identities,

$$2\,\cos(x) = (e^{i\,x} + e^{-i\,x}) \tag{A.14}$$

$$2\,\sin(x) = -i\,(e^{i\,x} - e^{-i\,x}) \tag{A.15}$$

then this equation can be re-written as the real equation,

$$v(t) = 2\,(0.4753 * \cos(1.7544\,t) - 0.7928 * \sin(1.7544\,t))\,e^{-1.8389\,t} - 1.9507\,e^{-2.3222\,t} + 1 \quad \text{(A.16)}$$

Note that $v(t = 0) = 0$ and $v(t = \infty) = 1$, as expected for a unity voltage step-function input signal. A graph of equation A.16 versus time, generated by Matlab's `ezplot()` command, is shown in figure A.1.

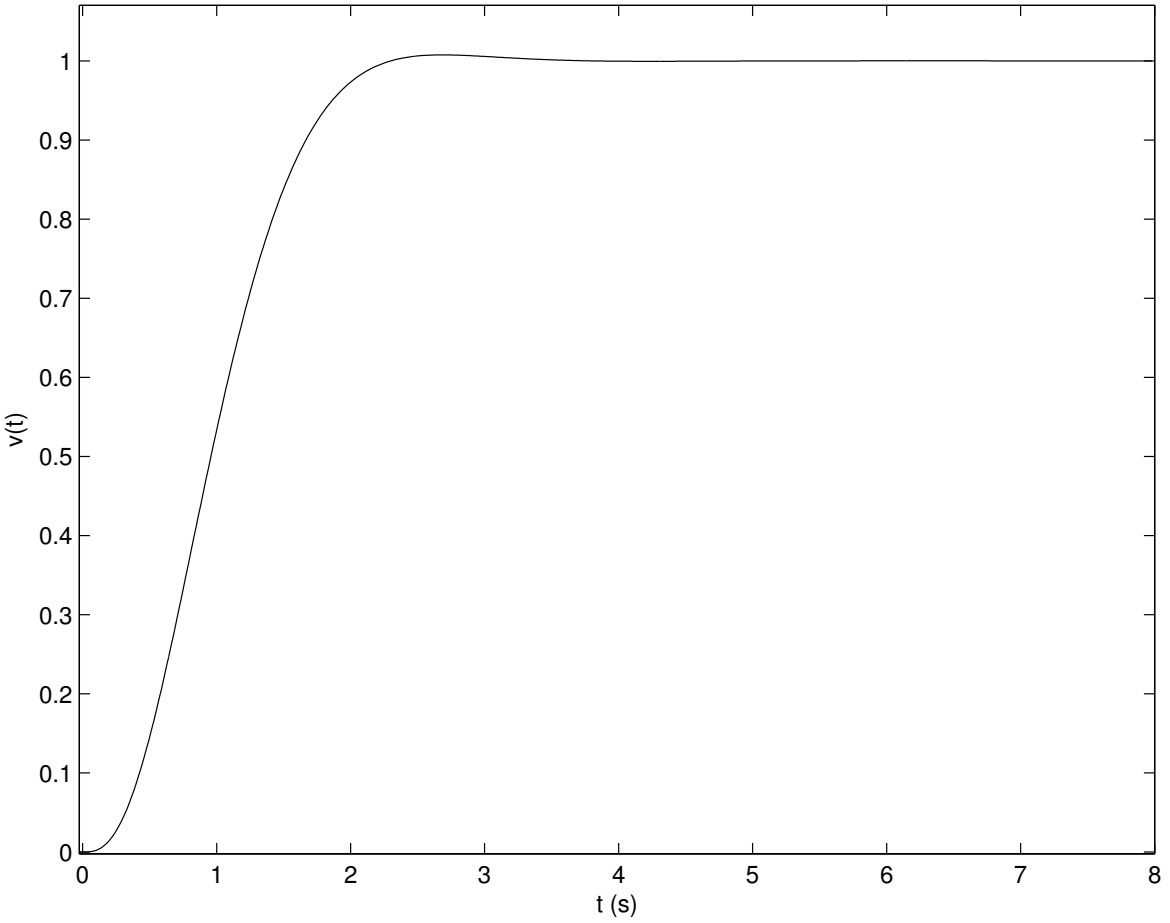

Figure A.1: The step-response of a delay-normalized 3-pole Bessel filter

To determine how long it takes for the step response to settle to within 0.02% of its final value of unity, the following loop in Matlab searches backward from 10s to the latest time at which the response deviates from unity by more than 0.02% of unity.

```
for x=10:-0.01:0,if(abs(1-subs(v,t,x)) > 0.0002), disp(x), break, end, end
```

This yields the value 4.98, indicating that following a step-function input, the output of a delay-normalized 3-pole Bessel filter settles to within 0.02% of its final value within 4.98s. For a filter designed to have a 3dB cutoff frequency of ω_{3dB}, the settling time to 0.02% is then given by

$$t_{0.02\%} = 4.98 * \frac{\Omega_{3dB}}{\omega_{3dB}} = 4.98 * \frac{1.756}{\omega_{3dB}}. \tag{A.17}$$

Thus a 2MHz 3-pole Bessel filter settles to 0.02% of its final value within 0.7μs of a step in the input signal.

A.4 Computing the time-constant of a Bessel filter

According to [Rohlfs (2000)], the time-constant, τ, to use for a low-pass filter that follows a square-law detector, is given by equation A.18.

$$\tau = \frac{|H(0)|^2}{\int_{-\infty}^{+\infty} |H(f)|^2 \, df} \tag{A.18}$$

Where f is the frequency in Hz. Since Matlab's symbolic math toolkit isn't able to perform the integration in the denominator, one has to resort to numerical integration to compute τ. To do this in Matlab one first has to create an *M-file* script containing the definition of a function that takes a single argument and returns a single value. The single argument is the dependent variable of the integration, and the return value is the corresponding value of the function being integrated. For convenience, and to avoid numerical problems of large numbers being raised to high powers, it is prudent to evaluate the integral for a hypothetical filter with a 1Hz 3dB cutoff frequency and then denormalize the result for the actual filter. Thus, starting from equation A.3, together with the renormalization factor of equation A.4, one creates a script in the matlab path (see `help addpath`), called (for example) `bess3sqrmod.m`. This file contains the following lines.

```
function y = bess3sqrmod(f)
 syms s;
 hh3 = 225./(-s.^6 + 6.*s.^4 - 45.*s.^2 + 225);
 y = subs(hh3, s, i.*1.756.*f);
```

This function returns the power gain of a filter with a 1Hz 3dB point, at a given frequency, f, expressed in Hz. Using this one then computes τ by integrating over the range of f for which `hh` is significantly non-zero, by typing:

```
tau = bess3sqrmod(0)/quad(@bess3sqrmod, -100, 100)
```

This yields the value 0.4658. Thus the time-constant for a 3-pole Bessel filter with a 3dB cutoff frequency of 2MHz is given by:

$$\tau = 0.4658/2e6 = 2.329e-7s = 0.23\mu\text{s} \tag{A.19}$$

A.5 Bessel filter equations and parameters

The Bessel-filter calculation procedures detailed in the preceding sections of this appendix were applied to all Bessel filters in the range 1 to 10 poles. The equations and parameters that resulted from these procedures are listed, per-filter, in the following sections. Note that the filter transfer functions shown, are those of delay-normalized filters, but these can be converted to any cutoff frequency by using the Ω_{3dB} parameter, as described earlier. The numbers that emerge from these equations for a 3dB cutoff frequency of 2MHz are those presented earlier in table 2.2.

A.5.1 The 1-pole Bessel filter

$$H(s) = \frac{1}{s+1} \tag{A.20}$$

$$|H(s)|^2 = \frac{1}{-s^2+1} \tag{A.21}$$

$$|H(\omega)|^2 = \frac{1}{\omega^2+1} \tag{A.22}$$

$$\Omega_{3db} = 1.0 \text{ rad}\, s^{-1} \tag{A.23}$$

$$Delay = \frac{1.0}{\omega_{3dB}} \tag{A.24}$$

$$v(t) = 1 - e^{-t} \tag{A.25}$$

$$t_{0.02\%} = 8.51\frac{\Omega_{3dB}}{\omega_{3dB}} = \frac{8.51}{\omega_{3dB}} \tag{A.26}$$

$$\tau = \frac{0.3203}{f_{3dB}} \tag{A.27}$$

A.5.2 The 2-pole Bessel filter

$$H(s) = \frac{3}{s^2 + 3\,s + 3} \tag{A.28}$$

$$|H(s)|^2 = \frac{9}{s^4 - 3\,s^2 + 9} \tag{A.29}$$

$$|H(\omega)|^2 = \frac{9}{\omega^4 + 3\,\omega^2 + 9} \tag{A.30}$$

$$\Omega_{3db} = 1.362 \text{ rad}\,s^{-1} \tag{A.31}$$

$$Delay = \frac{1.362}{\omega_{3dB}} \tag{A.32}$$

$$v(t) = 1 - (\cos(0.866\,t) + 1.7320\,\sin(0.866\,t))\,e^{-1.5\,t} \tag{A.33}$$

$$t_{0.02\%} = 5.84\frac{\Omega_{3dB}}{\omega_{3dB}} = \frac{7.95}{\omega_{3dB}} \tag{A.34}$$

$$\tau = \frac{0.4335}{f_{3dB}} \tag{A.35}$$

A.5.3 The 3-pole Bessel filter

$$H(s) = \frac{15}{s^3 + 6s^2 + 15s + 15} \tag{A.36}$$

$$|H(s)|^2 = \frac{225}{-s^6 + 6\,s^4 - 4\,s^2 + 225} \tag{A.37}$$

$$|H(\omega)|^2 = \frac{225}{\omega^6 + 6\,\omega^4 + 4\,\omega^2 + 225} \tag{A.38}$$

$$\Omega_{3db} = 1.756 \text{ rad}\,s^{-1} \tag{A.39}$$

$$Delay = \frac{1.756}{\omega_{3dB}} \tag{A.40}$$

$$v(t) = (0.9506\,\cos(1.7544\,t) - 1.5856\,\sin(1.7544\,t))\,e^{-1.8389\,t} + \tag{A.41}$$
$$-1.9507\,e^{-2.3222\,t} + 1$$

$$t_{0.02\%} = 4.98\frac{\Omega_{3dB}}{\omega_{3dB}} = \frac{8.7449}{\omega_{3dB}} \tag{A.42}$$

$$\tau = \frac{0.4658}{f_{3dB}} \tag{A.43}$$

A.5.4 The 4-pole Bessel filter

$$H(s) = \frac{105}{s^4 + 10\,s^3 + 45\,s^2 + 105\,s + 105} \tag{A.44}$$

$$|H(s)|^2 = \frac{11025}{s^8 - 10\,s^6 + 135\,s^4 - 1575\,s^2 + 11025} \tag{A.45}$$

$$|H(\omega)|^2 = \frac{11025}{\omega^8 + 10\,\omega^6 + 135\,\omega^4 + 1575\,\omega^2 + 11025} \tag{A.46}$$

$$\Omega_{3db} = 2.114 \text{ rad}\,s^{-1} \tag{A.47}$$

$$Delay = \frac{2.114}{\omega_{3dB}} \tag{A.48}$$

$$v(t) = (1.6474\,\cos(2.6574\,t) + 0.0524\,\sin(2.6574\,t))\,e^{-2.1038\,t} + (-2.6474\,\cos(0.8672\,t) - 5.0054\,\sin(0.8672\,t))\,e^{-2.8962\,t} + 1 \tag{A.49}$$

$$t_{0.02\%} = 3.92\frac{\Omega_{3dB}}{\omega_{3dB}} = \frac{8.2869}{\omega_{3dB}} \tag{A.50}$$

$$\tau = \frac{0.4779}{f_{3dB}} \tag{A.51}$$

A.5.5 The 5-pole Bessel filter

$$H(s) = \frac{945}{s^5 + 15s^4 + 105s^3 + 420s^2 + 945s + 945} \tag{A.52}$$

$$|H(s)|^2 = \frac{893025}{-s^{10} + 15s^8 - 315s^6 + 6300\,s^4 - 99225\,s^2 + 893025} \tag{A.53}$$

$$|H(\omega)|^2 = \frac{893025}{\omega^{10} + 15\omega^8 + 315\omega^6 + 6300\,\omega^4 + 99225\,\omega^2 + 893025} \tag{A.54}$$

$$\Omega_{3db} = 2.427\ \mathrm{rad}\,s^{-1} \tag{A.55}$$

$$Delay = \frac{2.427}{\omega_{3dB}} \tag{A.56}$$

$$v(t) = (0.6640\,\cos(3.571\,t) + 1.2744\,\sin(3.571\,t))\,e^{-2.3247\,t} + (4.0570\,\cos(1.7427\,t) - 5.8940\,\sin(1.7427\,t))\,e^{-3.3520\,t} + -5.7211\,e^{-3.6467\,t} + 1 \tag{A.57}$$

$$t_{0.02\%} = 3.81\frac{\Omega_{3dB}}{\omega_{3dB}} = \frac{9.2469}{\omega_{3dB}} \tag{A.58}$$

$$\tau = \frac{0.4814}{f_{3dB}} \tag{A.59}$$

A.5.6 The 6-pole Bessel filter

$$H(s) = \frac{10395}{s^6 + 21s^5 + 210s^4 + 1260s^3 + 4725s^2 + 10395s + 10395} \tag{A.60}$$

$$|H(s)|^2 = 108056025/(s^{12} - 21s^{10} + 630s^8 - 18900s^6 + 496125\,s^4 + -9823275\,s^2 + 108056025) \tag{A.61}$$

$$|H(\omega)|^2 = 108056025/(\omega^{12} + 21\omega^{10} + 630\omega^8 + 18900\omega^6 + 496125\,\omega^4 + 9823275\,\omega^2 + 108056025) \tag{A.62}$$

$$\Omega_{3db} = 2.703\ \mathrm{rad}\,s^{-1} \tag{A.63}$$

$$Delay = \frac{2.703}{\omega_{3dB}} \tag{A.64}$$

$$v(t) = (-0.6698\,\cos(4.4927\,t) + 1.0350\,\sin(4.4927\,t))\,e^{-2.5159\,t} + (8.2608\,\cos(2.6263\,t) + 0.9924\,\sin(2.6263\,t))\,e^{-3.7357\,t} + (-8.5910\,\cos(0.8675\,t) - 16.8060\,\sin(0.8675\,t))\,e^{-4.2484\,t} + 1 \tag{A.65}$$

$$t_{0.02\%} = 3.38\frac{\Omega_{3dB}}{\omega_{3dB}} = \frac{9.1361}{\omega_{3dB}} \tag{A.66}$$

$$\tau = \frac{0.4814}{f_{3dB}} \tag{A.67}$$

A.5.7 The 7-pole Bessel filter

$$H(s) = 135135/(s^7 + 28s^6 + 378s^5 + 3150s^4 + 17325s^3 + 62370s^2 + 135135s + 135135) \tag{A.68}$$

$$|H(s)|^2 = 18261468225/(-s^{14} + 28s^{12} - 1134s^{10} + 47250s^8 + -1819125s^6 + 58939650s^4 - 1404728325s^2 + 18261468225) \tag{A.69}$$

$$|H(\omega)|^2 = 18261468225/(+\omega^{14} + 28\omega^{12} + 1134\omega^{10} + 47250\omega^8 + 1819125\omega^6 + 58939650\omega^4 + 1404728325\omega^2 + 18261468225) \tag{A.70}$$

$$\Omega_{3db} = 2.952\ \mathrm{rad}\,s^{-1} \tag{A.71}$$

$$Delay = \frac{2.952}{\omega_{3dB}} \tag{A.72}$$

$$v(t) = (-1.0434\,\cos(5.4207\,t) - 0.0570\,\sin(5.4207\,t))\,e^{-2.6857\,t} + (3.2844\,\cos(3.5172\,t) + 8.5328\,\sin(3.5172\,t))\,e^{-4.0701\,t} + (16.1582\,\cos(1.7393\,t) - 22.2502\,\sin(1.7393\,t))\,e^{-4.7583\,t} + -19.3992\,e^{-4.9718\,t} + 1 \tag{A.73}$$

$$t_{0.02\%} = 3.03\frac{\Omega_{3dB}}{\omega_{3dB}} = \frac{8.9446}{\omega_{3dB}} \tag{A.74}$$

$$\tau = \frac{0.4803}{f_{3dB}} \tag{A.75}$$

A.5.8 The 8-pole Bessel filter

$$H(s) = 2027025/(s^8 + 36s^7 + 630s^6 + 6930s^5 + 51975s^4 + 270270s^3 + 945945s^2 + 2027025s + 2027025) \tag{A.76}$$

$$|H(s)|^2 = 4108830350625/(s^{16} - 36s^{14} + 1890s^{12} - 103950s^{10} + 5457375s^8 - 255405150s^6 + 9833098275s^4 + \tag{A.77}$$

$$
\begin{aligned}
& -273922023375s^2 + 4108830350625) \\
|H(\omega)|^2 &= 4108830350625/(\omega^{16} + 36\omega^{14} + 1890\omega^{12} + 103950\omega^{10} + \qquad (A.78)\\
& 5457375\omega^8 + 255405150\omega^6 + 9833098275\omega^4 + \\
& 273922023375\omega^2 + 4108830350625) \\
\Omega_{3db} &= 3.1796 \text{ rad}\, s^{-1} \qquad (A.79)\\
Delay &= \frac{3.1796}{\omega_{3dB}} \qquad (A.80)\\
v(t) &= (-0.3958\, \cos(6.3539\, t) - 0.7826\, \sin(6.3539\, t))\, e^{-2.8390\, t} + \qquad (A.81)\\
& (-6.3008\, \cos(4.4144\, t) + 7.2958\, \sin(4.4144\, t))\, e^{-4.3683\, t} + \\
& (36.3412\, \cos(2.6162\, t) + 5.7324\, \sin(2.6162\, t))\, e^{-5.2048\, t} + \\
& (-30.6446\, \cos(0.8676\, t) - 61.0486\, \sin(0.8676\, t))\, e^{-5.5879\, t} + \\
& 1 \\
t_{0.02\%} &= 2.77\frac{\Omega_{3dB}}{\omega_{3dB}} = \frac{8.8075}{\omega_{3dB}} \qquad (A.82)\\
\tau &= \frac{0.4789}{f_{3dB}} \qquad (A.83)
\end{aligned}
$$

A.5.9 The 9-pole Bessel filter

$$
\begin{aligned}
H(s) &= 34459425/(s^9 + 45s^8 + 990s^7 + 13860s^6 + 135135s^5 + 945945s^4 + \qquad (A.84)\\
& 4729725s^3 + 16216200s^2 + 34459425s + 34459425) \\
|H(s)|^2 &= 1187451971330625/(-s^{18} + 45s^{16} - 2970s^{14} + 207900s^{12} + \qquad (A.85)\\
& -14189175s^{10} + 893918025s^8 - 49165491375s^6 + \\
& 2191376187000s^4 - 69850115960625s^2 + 1187451971330625) \\
|H(\omega)|^2 &= 1187451971330625/(+\omega^{18} + 45\omega^{16} + 2970\omega^{14} + 207900\omega^{12} + \qquad (A.86)\\
& 14189175\omega^{10} + 893918025\omega^8 + 49165491375\omega^6 + \\
& 2191376187000\omega^4 + 69850115960625\omega^2 + 1187451971330625) \\
\Omega_{3db} &= 3.3917 \text{ rad}\, s^{-1} \qquad (A.87)\\
Delay &= \frac{3.3917}{\omega_{3dB}} \qquad (A.88)\\
v(t) &= (0.3984\, \cos(7.2915\, t) - 0.6120\, \sin(7.2915\, t))\, e^{-2.9793\, t} + \qquad (A.89)\\
& (-9.6128\, \cos(5.3173\, t) - 2.1238\, \sin(5.3173\, t))\, e^{-4.6384\, t} + \\
& (14.4600\, \cos(3.4982\, t) + 43.9100\, \sin(3.4982\, t))\, e^{-5.6044\, t} + \\
& (64.6624\, \cos(1.7378\, t) - 86.5320\, \sin(1.7378\, t))\, e^{-6.1294\, t} + \\
& -70.9080\, e^{-6.2970\, t} + 1 \\
t_{0.02\%} &= 2.56\frac{\Omega_{3dB}}{\omega_{3dB}} = \frac{8.6828}{\omega_{3dB}} \qquad (A.90)
\end{aligned}
$$

$$\tau = \frac{0.4776}{f_{3dB}} \tag{A.91}$$

A.5.10 The 10-pole Bessel filter

$$\begin{aligned}
H(s) &= 654729075/(s^{10} + 55s^9 + 1485s^8 + 25740s^7 + 315315s^6 + \\
&\quad 2837835s^5 + 18918900s^4 + 91891800s^3 + 310134825s^2 + \\
&\quad 654729075s + 654729075) && \text{(A.92)} \\
|H(s)|^2 &= 428670161650355648/(s^{20} - 55s^{18} + 4455s^{16} - 386100s^{14} + \\
&\quad 33108075s^{12} - 2681754075s^{10} + 196661965500s^8 + \\
&\quad -12417798393000s^6 + 628651043645625s^4 + \\
&\quad -22561587455281875s^2 + 428670161650355625) && \text{(A.93)} \\
|H(\omega)|^2 &= 428670161650355648/(\omega^{20} + 55\omega^{18} + 4455\omega^{16} + 386100\omega^{14} + \\
&\quad 33108075\omega^{12} + 2681754075\omega^{10} + 196661965500\omega^8 + \\
&\quad 12417798393000\omega^6 + 628651043645625\omega^4 + \\
&\quad 22561587455281875\omega^2 + 428670161650355625) && \text{(A.94)} \\
\Omega_{3db} &= 3.5910 \text{ rad } s^{-1} && \text{(A.95)} \\
Delay &= \frac{3.5910}{\omega_{3dB}} && \text{(A.96)} \\
v(t) &= (0.60 \cos(8.2327\,t) + 0.02 \sin(8.2327\,t))\, e^{-3.1089\,t} + \\
&\quad (-2.72 \cos(6.2250\,t) - 9.42 \sin(6.2250\,t))\, e^{-4.8862\,t} + \\
&\quad (-38.72 \cos(4.3849\,t) + 39.54 \sin(4.3849\,t))\, e^{-5.9675\,t} + \\
&\quad (155.30 \cos(2.6116\,t) + 27.74 \sin(2.6116\,t))\, e^{-6.6153\,t} + \\
&\quad (-115.48 \cos(0.8677\,t) - 232.66 \sin(0.8677\,t))\, e^{-6.9220\,t} + \\
&\quad 1.00 && \text{(A.97)} \\
t_{0.02\%} &= 2.39\frac{\Omega_{3dB}}{\omega_{3dB}} = \frac{8.5825}{\omega_{3dB}} && \text{(A.98)} \\
\tau &= \frac{0.4766}{f_{3dB}} && \text{(A.99)}
\end{aligned}$$

Appendix B

The power management circuit

The main properties of the power-management circuit have already been described in section 3.6. A diagram of this circuit is shown in figure B.1.

This consists of an off-the-shelf power-monitoring chip, the MAX6339, which pulls its $\overline{\text{RESET}}$ output low when any of its inputs fall below specific threshold voltages, and a transistor which uses this signal to switch a 10A 4-pole relay, to turn the CCB power on and off.

B.1 Interfacing to the voltage-monitor inputs

The MAX6339 comes in a number of versions, each designed for monitoring different sets of power-supply voltages. Naturally, none of these sets match all of the CCB power-supply voltages. However it is possible to monitor other input voltages, by using voltage dividers to make the actual power-supply voltages conform to the expectations of the chip. This has to be done with some care to ensure that component tolerances and the loading of the voltage dividers by the input pins, can't push the presented voltages too close to, or below the shutdown thresholds. This is complicated by the fact that each of the input pins is documented to draw a different current.

Originally the MAX6339MUT was chosen because its 5V and -5V monitor inputs matched two of the power supply voltages of the CCB. Since then the need for a -5V power supply has been dropped, and since the chosen MAX6339 needed a negative power-supply voltage at its IN4 input, a different version of the MAX6339 has had to be selected. The nearest equivalent that doesn't require a negative voltage at any of its inputs is the MAX6339EUT. In the modified circuit using this chip, IN4 is used to monitor the +12V signal that used to be monitored by IN3 of the MAX6339MUT, and IN3, which isn't used for monitoring, is tied to IN1 to prevent it from floating below its 2.5V threshold and turning off the power.

While the +5V analog power-supply voltage can be monitored directly by the IN1 input of

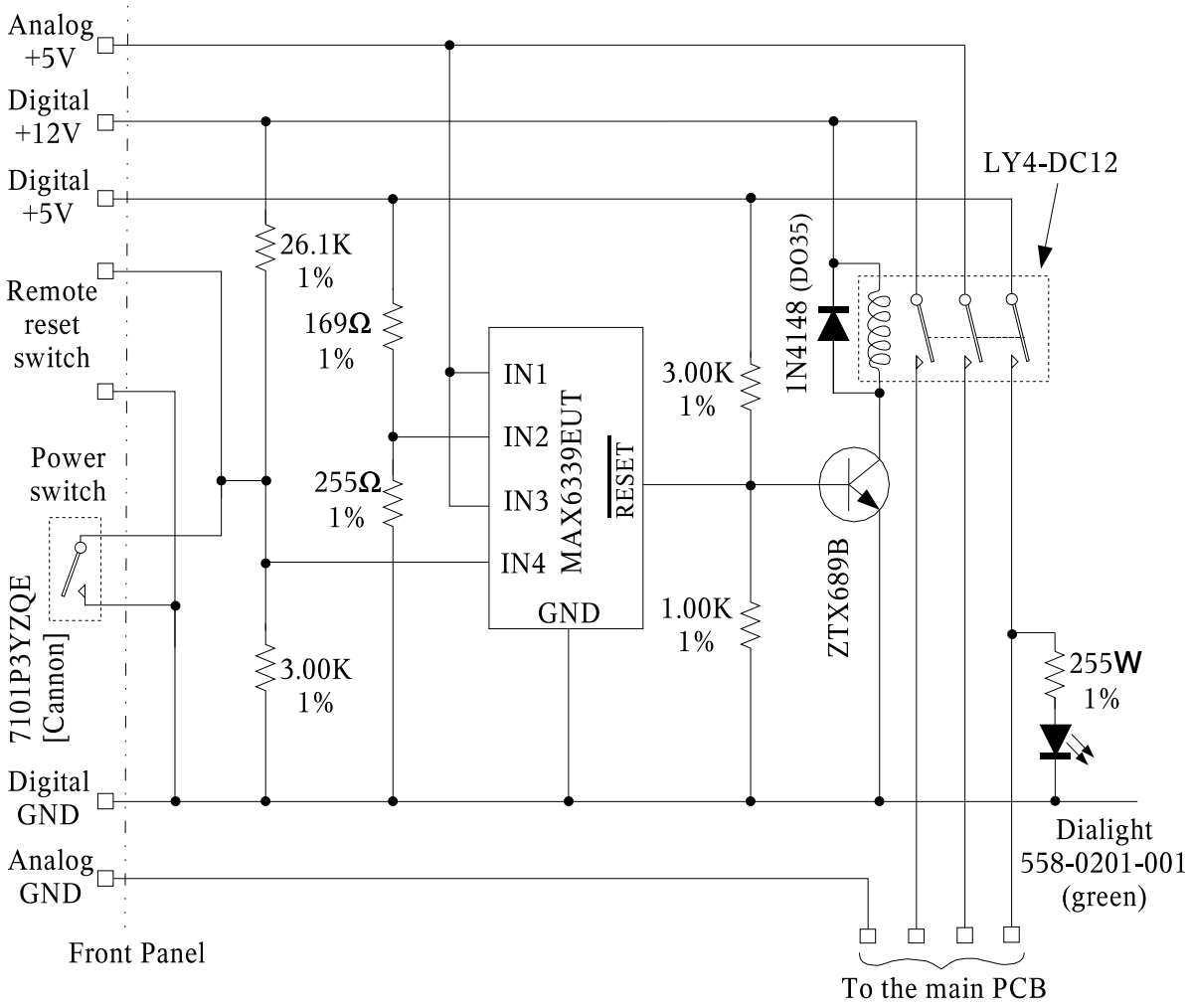

Figure B.1: The power-management circuit and its front-panel power switch

the MAX6339EUT, the digital +5V and +12V power supplies has to be accommodated by using voltage dividers at the other two monitor inputs. Of the latter two inputs, the 115μA maximum current drain of pin IN2 which expects 3V, is a thousand times greater than the 0.1μA maximum current drain of pin IN4, which expects just 1.23V, so it makes sense to use pin IN2 to monitor the 5V supply, which is closer to the target 3V, and pin IN4 to monitor the 12V supply.

In order not to compromise the stability of the threshold voltage on pin IN2, the potential divider applied to pin IN2 has to be stiff enough that variations in the 115μA current drain of the input pin can't change the divided voltage by more than about a percent. Thus the current flowing through the lower of the two resistors must be at least 100 times 115μA, or 11.5mA. Given the target input voltage of 3V, this implies that a resistor of no more than 261Ω be used for the lower of the two resistors in the potential divider. The corresponding upper resistor should be $(5V-3V)/3V$ or $1/6th$ of this value. Using the standard 1% resistor values, 255Ω and 169Ω, as shown in the circuit diagram, achieves this goal to within 2.5%, after taking into account the resistor tolerances. When the uncertainties in the IN2 current drain are added to this, the maximum error in the cutoff voltage on pin IN2 is about 3.5%. Since the chosen monitoring chip sets the cutoff thresholds at 10% below the power supply voltage, this is well within an acceptable margin.

Pin IN4 is easier to handle, due to its extremely small 0.1μA current drain. This current isn't enough to significantly load any practical voltage divider, so the requirements of the voltage divider are simply that the ratio of the uppermost to the lowermost of the resistors of the voltage divider be within a few percent of $(12V-1.23V)/1.23V = 8.756$, and that the resistors be small enough that capacitive pickup not be a potential problem. In the event, since the, shortly to be described, transistor bias circuit uses a $3.00K, 1\%$ resistor, and these resistors have to be bought in lots of 10, it made sense to choose this same value for the lower of the two resistors. The upper resistor, with a 1% resistance of $26.1K$, thus produces a ratio which is within 2.6% of the target ratio, after taking account of the resistor tolerances. Again, this is well within the 10% margin.

B.2 Interfacing a relay to the monitor output

The $\overline{\text{RESET}}$ output of the MAX6339EUT is not directly suitable for interfacing to a relay. It can only source 6μA when in its high output state, and can only sink up to an absolute maximum of 20mA when in its low state. The relay needs to be switched on when the $\overline{\text{RESET}}$ output is in its high state, whereas in this state the $\overline{\text{RESET}}$ output is unable to either source anything approaching enough current, or present a high enough voltage to turn on a relay.

Even with an external transistor, the measly 6μA available when the $\overline{\text{RESET}}$ is high, would be insufficient to draw enough current through the relay, so an external pull-up resistor to the digital 5V supply has to be added. To avoid destroying the chip, this pull-up must be of a value large enough not to require the MAX6339 to sink more than a fraction of the 20mA

absolute maximum, when the $\overline{\text{RESET}}$ pin is in its low state. Using 5mA as a reasonable maximum, this implies that the pull-up must be at least 1K.

The MAX6339 only guarantees that it can hold the $\overline{\text{RESET}}$ low when either of pins IN1 and IN2 are above 1V, so in addition to ensuring that we have enough current to drive the base of the relay driving transistor when the $\overline{\text{RESET}}$ pin is high, we need to ensure that if the 5V supply voltage falls far enough that pin IN2 falls below 1V, that the transistor base voltage also fall below the voltage needed to turn it on. Otherwise, if the 5V digital supply went bad, but the 12V digital supply was still okay, the relay, which is powered from the 12V supply, would inappropriately switch on. Thus, in addition to a pull-up resistor to the 5V supply, we also need a pull-down resistor to ground. The voltage at IN2 falls to 1V when the 5V digital supply voltage falls to 1.7V. If the FET inside the MAX6339 turns off at this point, the voltage $\mathrm{V_b}$ at the base, provided that it is less than the base cutoff voltage, is given simply by the voltage divider formed by the pull-up and pull-down resistors, supplied by 1.7V. Thus, if the pull-up resistor is called R1 and the pull-down resistor R2, then the base voltage is given by,

$$\mathrm{V_b} = 1.7\frac{R2}{R1 + R2} \tag{B.1}$$

A value of $\mathrm{V_b} < 0.5\mathrm{V}$ would be below the cutoff voltage of any normal transistor, and well below the base saturation voltage. Thus a ratio R1/R2 > 2.4 would guarantee that the transistor would be turned off if the 5V digital supply voltage were to fall below 1.7V. For convenience, we will adopt the value R1/R2=3.

Next, we need to take account of the transistor current gain, β, and the relay coil current, $\mathrm{I_c}$. The required base current to generate this collector current, is clearly $\mathrm{I_b} = \mathrm{I_c}/\beta$, so the total current going through the pull-up resistor, when the $\overline{\text{RESET}}$ pin is in its high-impedance state, is the sum of this base current and the current drawn by the pull-down resistor. Given a base saturation voltage of $\mathrm{V_{bs}}$, which is the voltage needed to turn on the transistor fully, we thus have another relation for R1 and R2.

$$\frac{(5 - \mathrm{V_{bs}})}{R1} = \mathrm{I_c}/\beta + \frac{\mathrm{V_{bs}}}{R2} \tag{B.2}$$

Substituting the previously chosen value of R1/R2=3, results in the following equation for R1.

$$R1 = \frac{\beta}{\mathrm{I_c}}(5 - 4\mathrm{V_{bs}}) \tag{B.3}$$

The chosen 4-pole relay requires a coil current, $\mathrm{I_c}$, of 120mA. Most transistors that are capable of sinking this collector current have current gains of about 20, and saturation

voltages of about 1V. Thus R1 would have to be no more than 166Ω. Unfortunately a resistor of this size would require that the $\overline{\text{RESET}}$ sink 30mA when held low, and that is far in excess of its capabilities. Worse still, this resistance assumes that the transistor really does have a current gain of 20, whereas the current gain of bipolar transistors is not a good parameter to rely on, and is highly variable as a function of temperature, so a smaller resistor would be needed in practice.

One possible solution would be to replace the transistor with a Darlington pair, since this would square the current gain. The problem with this is that it also increases the saturation collector-emitter voltage drop by one base-emitter voltage drop, and that would probably stop the relay from working. It also increases the base turn-on voltage.

A better solution is the seemingly unique ZTX689B, which is sold as a single-transistor replacement for Darlington pairs. It has an extremely impressive minimum current gain, β, of 500 at a collector current of 0.1A, and can even handle up to 3A at only moderately reduced gain. The base-emitter saturation voltage, V_{bs} is 0.9V. Therefore the maximum value of R1 becomes a more reasonable 5.8K, which would only result in the $\overline{\text{RESET}}$ pin having to sink up to 0.86mA when in the low state. To ensure that the transistor gets fully switched on when the $\overline{\text{RESET}}$ is high, regardless of temperature variations in β, it makes sense to use a resistor of about half this maximum value. The most convenient nearby 1% resistor value that Mouser sells is 3.00KΩ. And the corresponding closest value to R1/3, for resistor R2 is 1.00KΩ.

B.3 Manual power switches

Both the main power switch on the front panel, and the remote momentary-action power-reset switch in the control room, turn off the CCB by fooling the MAX6339 into thinking that one of the power supplies that it is monitoring has gone bad. This causes the MAX6339 to pull its $\overline{\text{RESET}}$ pin low, and turn off the power relay. Both switches, which are wired in parallel, achieve this simply by pulling the IN4 voltage monitoring pin to ground when either of them is closed. Note that this means that when the main power switch is closed, the CCB will turn off, and remain off, regardless of the position of the remote reset switch. Also note that it isn't necessary to debounce these switches, since the MAX6339 is documented to latch its $\overline{\text{RESET}}$ output low for at least 140ms (typically 200ms) whenever any of the monitored power-supply voltages fall out of range.

Note that the switches only need to carry 0.5mA when closed, and only have 1.23V across them when open.

B.4 Parts

Part numbers for the power circuit are shown in table B.1.

Description	Mouser #	Manufacturer #	Price
26.1$K\Omega$ 1% 1/8W metal-film	270-26.1K	Xicon 270-26.1K	\$0.11 for 10
3.00$K\Omega$ 1% 1/8W metal-film	270-3.0K	Xicon 270-3.0K	\$0.11 for 10
1.00$K\Omega$ 1% 1/8W metal-film	270-1K	Xicon 270-1K	\$0.11 for 10
255Ω 1% 1/4W metal-film	271-255	Xicon 271-255	\$0.09 for 10
169Ω 1% 1/4W metal-film	271-169	Xicon 271-169	\$0.09 for 10
1N4148 diode	512-1N4148	Fairchild 1N4148	\$0.04
Green LED	645-558-0201-001	Dialight 558-0201-001	\$0.9
4-Pole 4PDT 12VDC relay	653-LY4-DC12	Omron LY4-DC12	\$12.07
NPN high-gain transistor	522-ZTX689B	Zetex ZTX689B	\$0.80
Voltage monitor chip	?	MAX6339EUT-T	?
SPDT flat-lever toggle switch	611-7101-021	ITT/Cannon 7101P3YZQE	\$5.41

Table B.1: Part numbers for the power-control circuit

Appendix C

The analog input circuit

This appendix describes the digitizer circuit that is duplicated for each of the 16 signals that arrive at the twinax inputs of the CCB. As previously specified, the signals arriving from the receiver are assumed to be balanced differential signals swinging over a 5V range, between -2.5V and +2.5V, with a common-mode voltage in the range 1.0V to 3.2V.

The proposed circuit is shown in figure C.1, and described in the following sections.

C.1 Impedance matching to the twinax cables

The 78Ω twinax cable is matched to the inputs of the AD8138 differential amplifier by the parallel resistance of the shown 84.5Ω matching resistor and the 998Ω input impedance of the differential amplifier. Note that, as described on page 10 of the AD8138 datasheet, the input impedance of the differential amplifier is given by the sum of the two leftmost feedback resistors

C.2 The differential amplifier feedback resistors

A side-effect of impedance matching the +/-5V differential outputs of the AD8138 in the receiver, is that the differential voltage arriving over the twinax cables is halved to a swing of 2.5V by the time that it reaches the inputs of the backend differential amplifier. This is half what is needed by the AD9240 ADC, so the feedback resistors of the backend AD8138 were chosen to amplify the input signal by a factor of 2. The equivalent resistors in the two feedback networks must be paired resistors with ratio tolerances of 0.01%, in order to maintain a high CMRR (common-mode rejection ratio), and achieve the optimal noise performance, as elaborated on page 10 of the AD8138 datasheet. To maintain this precision,

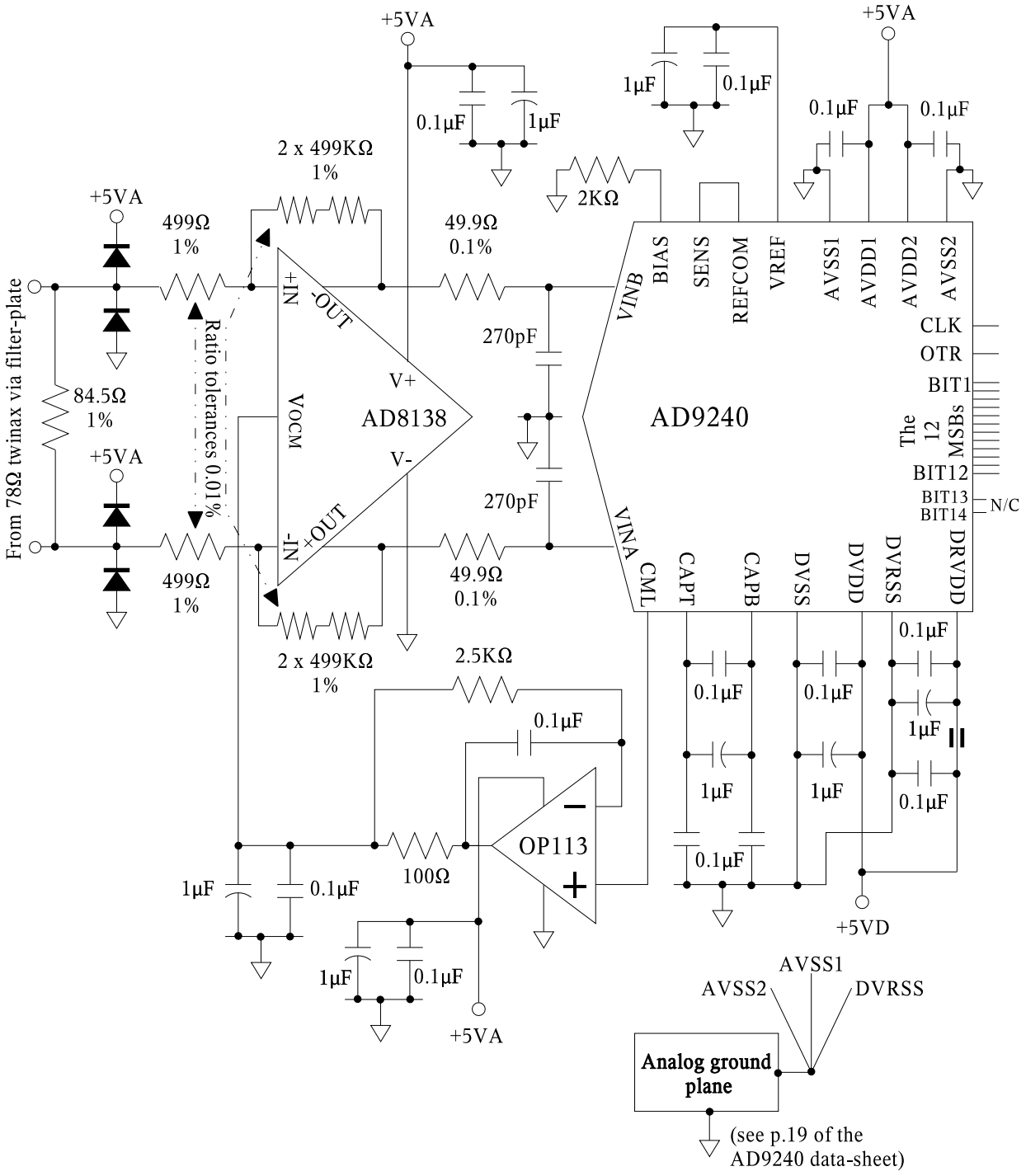

Figure C.1: Analog input circuit of one channel of the CCB

care will have to be taken that the PCB traces joining these to the respective sides of the AD8138 have the same lengths. Note the use of 6 equal-valued resistors in the two feedback networks, as suggested by John Ford, rather than two 499Ω series resistors and two $1K\Omega$ feedback resistors. This allows all of the resistors to be part of a single high-precision resistor array. Suitable resistor-arrays can be custom ordered from Vishay Dale. Note that whereas the relative tolerances of these resistors needs to be high, the absolute tolerance of their shared value can be as poor as 1%. The values of the feedback resistors were chosen according to table 1 in the AD8138 datasheet, to give the best noise performance and a gain of 2.

C.3 Clamping the outputs of the differential amplifier

In a previous rendition of the analog circuit, clamp diodes were included between the AD8138 outputs and the ADC inputs. These were needed because the AD8138 was to be powered from dual +5V and -5V supplies, the latter of which meant that the AD8138 could swing the voltage more negative than allowed by the inputs of the AD9240. In the current circuit, the AD8138 is powered by a single +5V power-supply, and is thus incapable of presenting voltages that the AD9240 can't handle. The clamping diodes have thus been removed.

C.4 Interfacing to the AD9240 inputs

The datasheet of the AD9240 suggests placing 50Ω resistors in series with its inputs, to isolate the differential driver from the variable input impedance presented by its accumulation capacitor. Higher resistor values can also be used, but apparently they result in higher distortion.

The AD9240 datasheet also recommends limiting the noise bandwidth by adding shunt capacitors between the two inputs and analog ground. When the capacitance of the chosen 270pF capacitors are summed with the 16pF input capacitance of the AD9240, the 3dB bandwidth of the low-pass filter that this forms with the 50Ω series resistors is just over 10MHz.

Using Matlab one finds that the combination of the main 2MHz low-pass filters in the receiver, followed by the single-pole 10MHz low-pass filters preceding the AD9240s, lengthens the settling time set by the 2MHz low pass filters from 0.7μs to 0.713μs, and increases the relative attenuation at 2MHz from 3dB to 3.2dB. This is acceptable, given the benefits of adding some rejection for out-of-band noise introduced between the main filters and the ADCs. Mica SMD capacitors have been selected for this purpose, since they don't have any resonances below a GHz, are stable, reliable, and have low inductances. Mouser and Newark only sell them with 5% tolerances, but since we have to buy at least 64 of them for the two

CCBs, it should be possible to hand-sort these by value, using a capacitance meter, and select well matching pairs.

C.5 Setting the common-mode ADC input level

The common mode voltage at the output of the AD8138 is set by the voltage at its V_{ocm} input. Unfortunately the AD8138 datasheet doesn't specify the input impedance of this pin. It does, however say that it should be driven by a low impedance source. The datasheet for the AD9240 is equally cagey about the characteristics of its common-mode output pin, CML, saying only that if used for any external biasing, it must be buffered. Thus, despite the fact that the datasheet for the AD8138 shows a couple of examples of other ADCs driving the AD8138 V_{ocm} pin directly with their CML outputs, I decided to play it safe and adopt the buffering circuit shown in the example of figure 34 in the AD9240 datasheet. This circuit looks odd, but basically it appears to be a simple op-amp follower circuit combined with a Pi low-pass filter.

C.6 Decoupling

In many places, pairs of 0.1μF and 1μF are used to decouple power supply and other DC lines. These are mostly according to the recommendations in the respective datasheets. The 0.1μF capacitors should be ceramic capacitors, whereas the 1μF capacitors should be tantalum beads.

The one place where the decoupling departs somewhat from the advice in the datasheets is that between the DRVDD DRVSS pins of the AD9240. I elected to try to improve on the decoupling by adding a ferrite bead between two of the capacitors to form a pi filter.

Note that the digital power-supply pin is decoupled to the analog ground plane, not the digital ground plane. This follows the advice in Analog Devices app-note [AN-280].

C.7 Other connections

The SENS and REFCOM pins are connected together to cause the AD9240 to use a 2.5V internal voltage reference, rather than an external reference voltage. The internal reference appears to be adequate. According to figure 19 of the AD9240 datasheet, over the temperature range of 20-30°C, the internal voltage reference will be stable to within about 0.02% of its value, which corresponds to our target 11-bit resolution. In an air-conditioned room, it should behave significantly better. The alternative of sharing a single external reference

between all ADCs seems attractive, but it would involve long PCB tracks to distribute this reference between the chips, and this would constitute a problematic circuit loop that would be liable to pick up interfering signals and cause crosstalk.

The BIAS pin of the AD9240 is connected to ground via a 2K resistor. This selects the normal operating speed of the ADC and the maximum SINAD. The effects of this and other resistor values are characterized in figures 21 and 22 of the AD9240 datasheet.

C.8 The ground planes

Page 19 of the AD9240 datasheet briefly discusses grounding issues. It says that all of the ground pins of the AD9240 must be connected together directly beneath the chip. As elaborated in Analog Devices app-note [AN-280], they should all be tied to the analog ground plane, and there should be no connections to the digital ground plane. The return path of the digital 5V supply of the ADC will thus pass through the analog ground plane to the single point at which the physical power-supplies where the digital and analog grounds are joined.

Note that this requirement only pertains to the ADC. All following digital circuit, such as the FPGA, obviously must be grounded and decoupled to the digital ground plane.

C.9 Choice of components

Wherever possible, surface-mount components have been selected. In addition to making the board more compact, this should simplify the PCB layout and reduce parasitic inductances.

C.10 Distortion

The THD (Total Harmonic Distortion) generated by the AD9240 depends on the input frequency and the voltage swing. For example, a 5V p-p, 5MHz input signal, generates a THD of -56dB, making the AD9240 equivalent to a 9-bit ADC. Fortunately, due to the 2MHz Bessel filters that follow the detectors in the receiver, 5MHz signals presented to the AD9240 by the CCB will be at most -23dB of the full-scale input swing, at which level the THD is well below detectable limits.

At 2MHz, according to figure 18 of the AD9240 datasheet, an input signal with a peak-to-peak swing of -0.5dB of the full-scale 5V input swing, has a THD of about -66dB, which corresponds precisely to our target resolution of 11-bits. Of course at this frequency the

Bessel filters in the receiver actually ensure that for the maximum signal that the CCB can handle before saturating, the signal-level at 2MHz will be -3dB of full-scale, so clearly, according to this graph distortion will again be below our detection threshold.

At still lower frequencies, the THD falls below our 11-bit detection limit regardless of the signal input swing.

Thus, provided that the ADC behaves as advertised, the THD of the AD9240 should not be detectable by the CCB, even for the strongest signals expected. If this turns out to be optimistic, then it shouldn't be a show stopper, because the fact that the spectrum of the thermal signal entering the CCB should always be the same for a given signal level, means that any distortion that is generated should be correctable in the FPGA via lookup tables that relate measured to true values.

C.11 Noise

The CCB design specification calls for up to 3 of the 11 bits of the ADC resolution be devoted to sampling the noise. Thus for a differential signal span of 5V at the inputs of the AD9240, the maximum differential RMS noise level arriving at the ADC inputs should not exceed $5/2^{11-3} = 19.5mV$.

For the chosen feedback resistors, table 1 in the AD8138 datasheet, indicates that the noise at the output of the AD8138, due to internal amplifier noise and Johnson noise from the feedback resistors, is 18.2nV/$sqrtHz$. The quadrature sum of this and the Johnson noise generated by the impedance matching resistor, R_{in} amplified by the signal gain, g, of the amplifier is given by,

$$e_{out}^2 = g^2 B_n((18.2 \times 10^{-9})^2 + 4KTR_{in}) \tag{C.1}$$

Where B_n is the noise bandwidth, K is Boltzmann's constant, and T is room temperature. The single-pole RC filters at the inputs of the ADC, each have 3dB bandwidths of about 10MHz. The corresponding equivalent noise bandwidth, B_n, is 1.57 times this, or 15.7MHz. Thus for $T = 295$K and $g = 2$, the total noise contribution of the CCB input stage comes to a total of $0.14mV$ RMS, which is less than 100th of the maximum tolerable noise level indicated above, and can safely be ignored.

Taking this further and assuming that the only significant noise contributors are the initial high-gain stages of the receiver, where the component-generated noise levels have similar magnitudes to the detected signals, and that the 2MHz low-pass filter is placed after these stages, the important noise bandwidth is actually 2MHz, rather than the 15.7MHz noise-bandwidth of the filters at the ADC inputs. Thus, given that the AD8138 input stage has a signal gain of 2, which implies that the maximum tolerable RMS noise level at the input

to the CCB is 19.5/2mV = 9.75mV, the maximum tolerable spectral noise density arriving from the receiver is $6.9\mu V/\sqrt{Hz}$, averaged over a 2MHz bandwidth.

C.12 Overall layout

Since neither the FPGA, nor the separate system monitoring ADCs have been specified yet, it isn't possible yet to layout the PCB. However a few characteristics can be described. As roughly shown in figure 1.1, the plan is to have a roughly central FPGA surrounded by a square annular analog section, with four analog channels arrayed along each side. The aim is to keep the lengths of the PCB traces that join the ADC outputs to the FPGA, as short and direct as possible, and as far away from the analog inputs as possible, and thus reduce the possibilities for coupling radiated digital signals back into the analog circuits. Just inside the four outer edges of the PCB, edge connectors that mate with the filtered plates of the input filter box, will be mounted, to carry the input signals to the analog circuit inputs. As previously mentioned, the chosen 14-pin filter plates will allow for 2 unused pins between each of the differential pairs, and thus reduce crosstalk and ease PCB layout.

Bibliography

[Blinchikoff (1976)] Blinchikoff, H. J. and Zverlev, A. I., *"Filtering in the Time and Frequency Domains"*, pages 147-148.

[Daniels (1974)] Daniels, R. W., *"Approximation methods for Electronic Filter Design"*, page 255.

[Dicke (1946)] Dicke, R. H., Rev. Sci. Instr., 17, 268-275 (1946)

[Mason (2002)] Mason, B. S, email, (Aug 31 2002).

[Rohlfs (2000)] Rohlfs, T. L. and Wilson, K., *"Tools of Radio Astronomy"*, 3rd Edn, 61-64, (2000).

[Su (2002)] Su, K. L., *"Analog Filters"*.

[AN-280] Analog Devices app-note 280, *"Mixed Signal Circuit Techniques"*
`http://www.analog.com/UploadedFiles/Application_Notes/561147779596939924617712O5AN280.pdf`